IP6557 application note

Version/Revision History

Version	Date	Comments	Author
V1.00	2023.03.01	Initial release	Ourunyu

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1. Typical Application Schematic

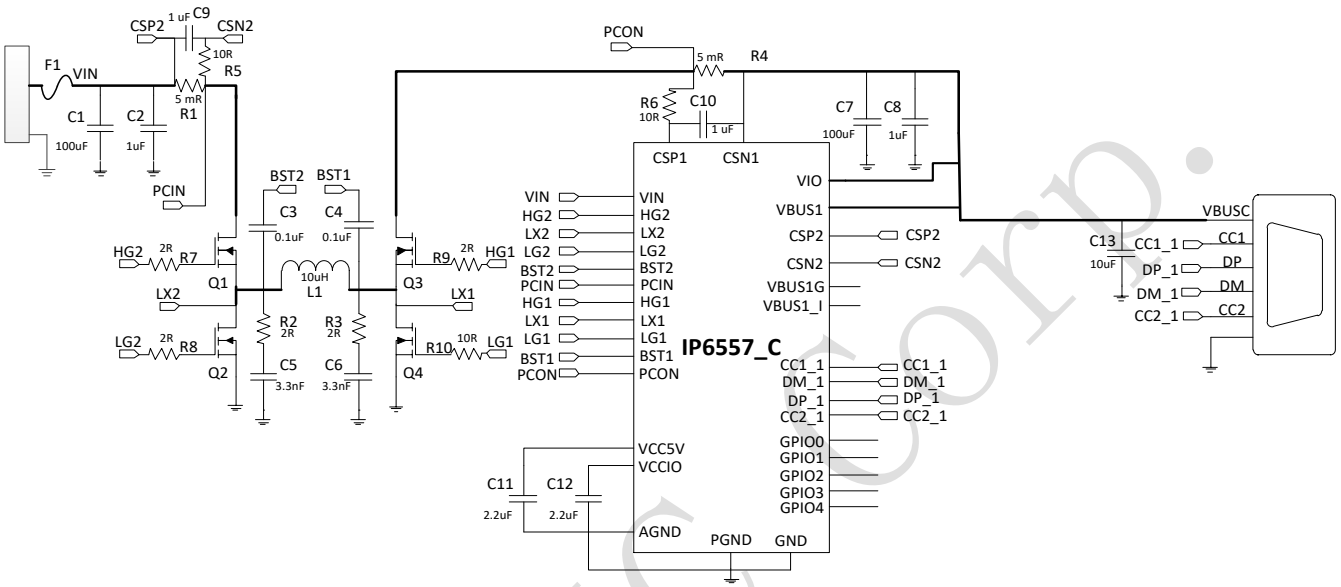

Figure 1 Typical application schematic diagram of IP6557 single C port

Notes:

1、The input capacitors C1 and C2 need to be placed between the input and the upper MOSFET Q1, and cannot be placed between the VIN PIN of the IC and the upper MOSFET Q1.

2、C1 is an electrolytic capacitor, used to absorb input spike voltage to protect IC.

3、C3 and C4 are bootstrap capacitors and need to be placed close to the LX and BST pins of the IC.

4、The capacitors of VCC5V and VCCIO are placed close to the device pin.

5、For the better ripple effect, it is recommended to use a 220uF/35V solid state capacitor for the output capacitor and add more 10uF ceramic capacitors at the output.

6、For the 100W output solution, VIN is recommended to be higher than 12V. For the 140W output solution, VIN is recommended to be higher than 20V.

2. Precautions for PCB layout

IP6557 integrates step-down controller. PCB layout is important for system stability, EMI, and other performance indicators. The PCB layout suggestions are as follows:

1. The loop composed of input capacitor and upper tube NMOS (controlled by HG2) and lower tube NMOS(controlled by LG2) should be as small as possible.

2. The loop composed of output capacitor and upper tube NMOS (controlled by HG1) and lower tube NMOS(controlled by LG1) should be as small as possible.

3. The inductor cable connecting the upper power tube and the lower power tube should be as wide and short as possible, so that the node area can ensure the maximum output current capacity.

4. The lines of HG1/LG1 and HG2/LG2 are parallel and the distance between those lines should be as wide as possible.

5. The loop composed of LX1/LX2 buffer circuit and PGND should be as small as possible.

6. The current sampling line for 5mohm resistance is directly drawn from both ends of the resistance（including PCON/CSP2/CSN2/PCIN/CSP1/CSN1）. The line is parallel, as short as possible and avoids LX/BST/HG/LG and other switching nodes.

7. The capacitance of VCC5V and VCCIO is placed close to the device PIN.

8. The GND of the input and output capacitors must be connected to the PGND of a large area.

9. For better ESD protection, it is recommended to reserve the positions of resistors in series and diodes to ground in the CC1/CC2/DP/DM lines, and reserve capacitors to ground in CC1/CC2.

Layout example:

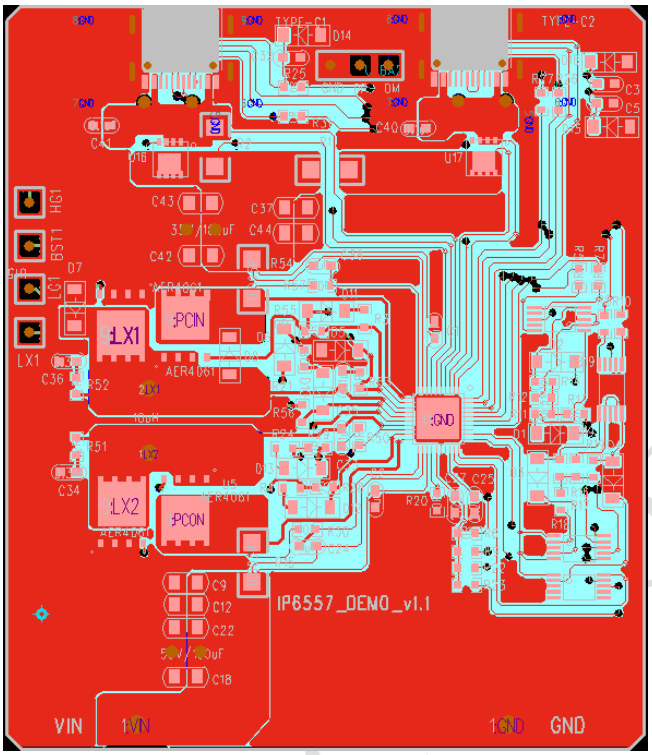

Figure 5 Front view of IP6557 DEMO board

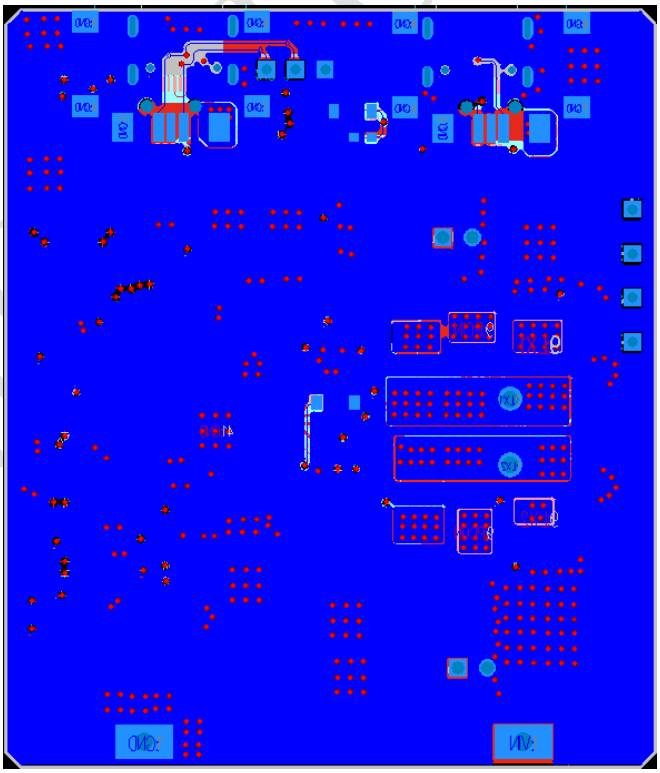

Figure 6 Bottom view of IP6557 DEMO board

3. EMI rectification suggestions

- **1.** The input ground, input capacitor ground, IC ground, output capacitor ground, and output receptacle ground should be directly connected in the same plane as far as possible.
- **2.** Switch signal LX traces are as short as possible, and too long traces will increase radiated energy.
- **3.** Input and output must add small ESR ceramic capacitors, the smaller the ground loop, the better. Adding ceramic capacitors at the input is more effective in improving EMI.
- **4.** If the structure allows, the inductor is best to lie flat to reduce the energy radiated into the air.
- **5.** For solutions with high EMI requirements, reserve the HG/LG resistor and diode bleeder path.
- **6.** For solutions with high EMI requirements, reserve circuits to connect the resistor in series with the BST capacitor.

4. Scheme description

IP6557 Single C port solution:

PDOs of IP6557_C for USB-C port: 5V/3A、9V/3A、12V/3A、15V/3A、20V/5A、ERP 28V/5A,
And two PPS : 3.3V-11V/3A、3.3V-21V/3A.
When current of PDO is higher than 3A, E-Marker wire is required to work.

PDO can be customized according to customer needs.

5. Application Notes

Input Capacitance Selection

The ESR of the input capacitor should be as small as possible. The ESR will affect the conversion efficiency of the system.

When the input voltage is significantly greater than the output voltage, the device works in buck mode.The maximum ripple current supported by the input capacitor must be greater than the maximum VIN ripple current of the system. The ripple current RMS value ($I_{RMS(VIN)}$) of the input capacitor is calculated as follows:

$$I_{RMS(VIN)} = I_{LOAD} * \sqrt{\frac{V_{OUT}}{V_{IN}} * (1 - \frac{V_{OUT}}{V_{IN}})}$$

I_{LOAD} is the load current, V_{IN} is the input voltage, V_{OUT} is the output voltage.

Inductance Selection

The inductor with 10uH is recommended for most applications.

The DCR of inductor has great influence on the conversion efficiency of the system, low DCR inductors are recommended. For solutions above 30W, it is recommended to use an inductor with a DCR of less than 10mohm.

The inductor saturation current should be at least 20% greater than the system's peak inductor current limit, in order to avoid inductance saturation, resulting in a decrease in inductance, system instability.

The calculation formula of the PEAK current ($I_{L(PEAK)-BUCK}$) in buck mode is as follows:

$$I_{L(PEAK)-BUCK} = I_{LOAD} + \frac{V_{OUT}*(V_{IN}-V_{OUT})}{2*V_{IN}*F_S*L}$$

The calculation formula of the PEAK current ($I_{L(PEAK)-BOOST}$) in boost mode is as follows:

$$I_{L(PEAK)-BOOST} = \frac{V_{OUT}*I_{LOAD}}{V_{IN}*EFF} + \frac{V_{IN}*(V_{OUT}-V_{IN})}{2*V_{OUT}*F_S*L}$$

I_{LOAD} is the LOAD current, V_{IN} is the input voltage, V_{OUT} is the output voltage, L is the inductance, F_S is the switching frequency，EFF is the conversion efficiency of DCDC.

Output Capacitance Selection

When the output voltage is significantly greater than the input voltage, the device works in boost mode.The maximum ripple current supported by the output capacitor must be greater than the maximum VOUT ripple current of the system. The ripple current RMS value ($I_{RMS(VOUT)}$) of the output capacitor is calculated as follows:

$$I_{RMS(VOUT)} = I_{LOAD} * \sqrt{\frac{V_{OUT}}{V_{IN}} - 1)}$$

I_{LOAD} is the load current, V_{IN} is the input voltage, V_{OUT} is the output voltage.

The output capacitance is used to keep the output stable. The value of ESR and capacitance has an effect on the output ripple.

The output ripple voltage $V_{OUT(RIPPLE)-BUCK}$ in buck mode can be calculated as follows:

$$V_{OUT(RIPPLE)-BUCK} = \frac{V_{OUT}*(V_{IN}-V_{OUT})}{V_{IN}*L*F_S} * (R_{ESR} + \frac{1}{8*F_S*C_{OUT}})$$

R_{ESR} is the equivalent serial resistance value of the output capacitance, F_S is the switching frequency, C_{OUT}

is the output capacitance value.

The output ripple voltage $V_{OUT(RIPPLE)-BOOST}$ in boost mode can be calculated as follows:

$$V_{OUT(RIPPLE)-BOOST} = \frac{I_{LOAD}*V_{OUT}*R_{ESR}}{V_{IN}} + \frac{(V_{OUT}-V_{IN})*I_{LOAD}}{V_{OUT}*F_S*C_{OUT}}$$

R_{ESR} is the equivalent serial resistance value of the output capacitance, F_S is the switching frequency, C_{OUT} is the output capacitance value.

MOSFET Selection

MOSFET devices that $V_{(BR)DSS}$ at least 20% higher than the input voltage are recommended.

$R_{DS(ON)}$ of MOSFET causes the power loss of the on-device, which has a direct impact ON the conversion efficiency of the system. Generally, it is recommended to choose a 10mohm MOSFET with $R_{DS(ON)}$.If the solution requires higher power output, lower $R_{DS(ON)}$ devices are recommended.

The C_{ISS} of MOSFET affects its switching speed. It is necessary to adjust the resistance of HG and LG in series according to different MOSFET, and adjust the driving speed of MOSFET to ensure the system stability. The MOSFET which its C_{ISS} value is less than 1000pF is advised to choose.

The RC buffer circuit of LX1/LX2 can suppress the burr of LX. The proper RC buffer circuit can make the system have better EMI effect.

For the circuit of the driving part, it is recommended to reserve HG1/HG2 and LG1/LG2 series resistors of 0603 specifications and RC buffer circuit as shown in the following figure.

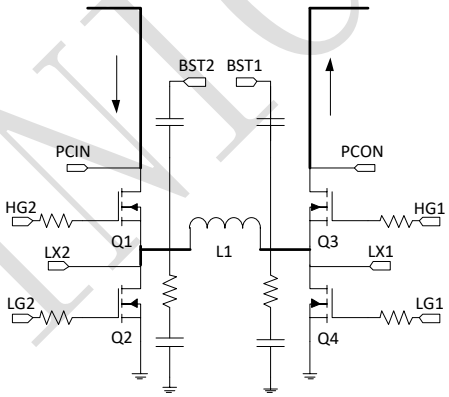

Figure 7 IP6557 MOSFET drive circuit diagram

6. IP6557 Series Product Introduction

Product	Introduction
IP6557_C	Single C port PD fast charge output.

Notes：

1、IP6557 supports a maximum power output of 140W (28V/5A).

2、IP6557 supports indicating its own status through IO/IIC or to control other modules in the solution, which is convenient to achieve multi-port solutions.

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