Programmable USB Type-C PD Controller

1 Features

- **USB TYPE-C Controller**
  - Cable Recognition
  - Supporting VCONN with Programmable OCP
  - Current Capability Definition and Detection
  - Attach/Detach Detection as Source, Sink or DRP
- **USB Power Delivery(PD) Controller**
  - Dual-Role PD Compatible
  - BIST Mode Supported
  - Supported PD 3.1 except Fast Role Swap Function
  - Biphase Mark Coding(BMC)
  - Physical Layer(PHY) Protocol
  - Policy Engine
  - Alternate Mode Support
- **Dead Battery Support**
- **VBUS detection**
- **Simple I2C Interface with INT pin**
- **Low Power Mode for Attach Detection**
- **9-Ball WL-CSP Package**
- **28V tolerance for VBUS/CC1/CC2**

2 Description

IP2751 is a USB Type-C PD controller that complies with the latest USB Type-C PD3.1 standards. It encapsulates VBUS detect and VCONN power control, USB Type-C CC logic, the USB PD BMC Physical Layer and portion of the USB PD Protocol Layer.

IP2751 integrates the USB Type-C Port Controller Interface(TCPCI) which is an I2C slave with INT_N signal for requesting attention and uses I2C to communicate with the TCPM.

3 Typical Applications

- **Smartphones**
- **Tablets**
- **Laptops**

4 Typical Application Schematic

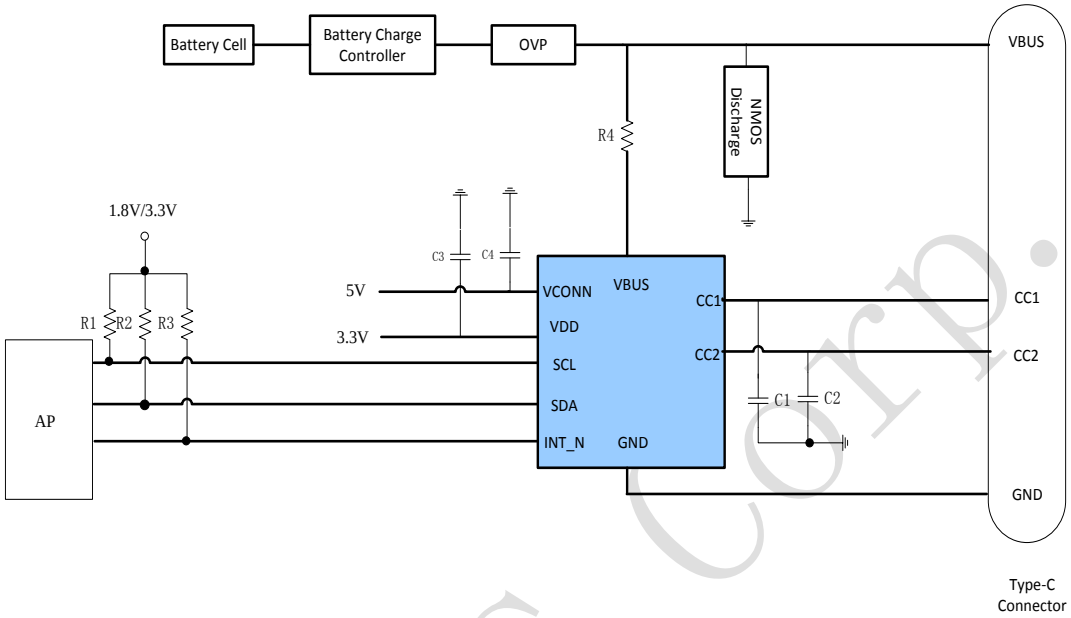


Table 1 Recommended Components Information

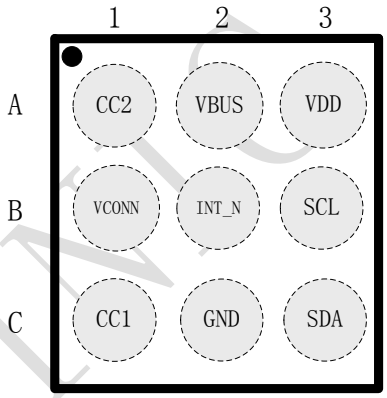
Reference	Description	Package
R1, R2, R3	1kΩ 1%	0402
R4	4.7kΩ 1%	0402
C1, C2	330pF/25V	0402
C3, C4	100nF/50V	0402

Table 2 Funtion Portfolio Information

Function Portfolio	Pin Name	Pin Connection
Use VCONN	VBUS	Short to connector VBUS or 4.7k to connector VBUS (better for surge)
	CC1	Short to connector CC1
	CC2	Short to connector CC2
	VCONN	Short to DC-DC2
	INT_N	Pull-high to AP
	SDA	Pull-high to AP
	SCL	Pull-high to AP
	VDD	Short to DC-DC1

Unused VCONN	VBUS	Short to connector VBUS or 4.7k to connector VBUS (better for surge)
	CC1	Short to connector CC1
	CC2	Short to connector CC2
	VCONN	Short to GND
	INT_N	Pull-high to AP
	SDA	Pull-high to AP
	SCL	Pull-high to AP
	VDD	Short to DC-DC1

5 PIN Description

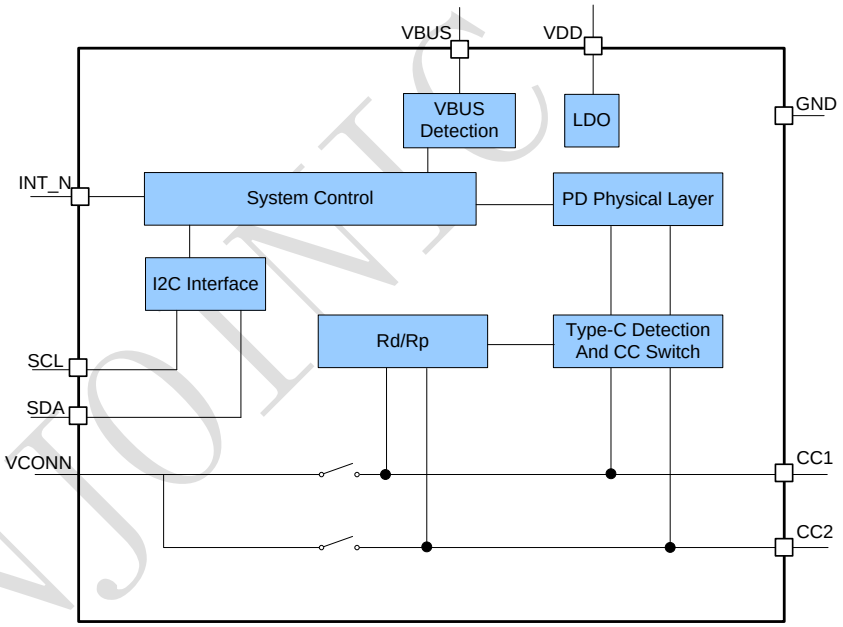


WL-CSP-9B 1.23*1.26 (BSC)

Pin No.	Pin name	Pin Function
A1	CC2	Type-C Connector Configuration Channel signal 2.
A2	VBUS	VBUS input pin for attach and detach detection.
A3	VDD	Input supply voltage.
B1	VCONN	Regulated input pin to be switched to correct CC pin as VCONN to power Type-C full-featured cables and other accessories.

B2	INT_N	Open drain type interrupt output. Asserted low to indicate status change occurred. Requires an external pull-up resistor.
B3	SCL	I2C serial clock signal to be connected to the I2C master. Requires an external pull-up resistor.
C1	CC1	Type-C Connector Configuration Channel signal 1.
C2	GND	Ground pin.
C3	SDA	I2C serial data signal to be connected to the I2C master. Requires an external pull-up resistor.

6 Internal Block Diagram



7 Absolute Maximum Ratings

Parameters	Symbol	Value	Unit
VDD/VCONN Input Voltage Range	VDD/VCONN	-0.3 ~ 6	V
VBUS Input Voltage Range	VBUS	-0.3 ~ 28	V
CC1，CC2 Input Voltage Range	V_{CC1}，V_{CC2}	-0.3 ~ 28	V
SCL/SDA/INT_N Input Voltage Range	V_{SCL}，V_{SDA}，V_{INT_N}	-0.3 ~ 6	V
Junction Temperature Range	T_J	-40 ~ 150	℃

Storage Temperature Range	Tstg	-60 ~ 150	℃
Lead Temperature Range (Soldering, 10sec)	Ts	260	℃
Ambient Temperature Range	T_A	-40~120	℃
Package Thermal Resistance	θ_{JA}	90	℃/W
Human Body Model (HBM) (SCL/SDA/INT)	ESD	3	KV
Human Body Model (HBM) (Other pin)	ESD	4	KV
Moisture Sensitivity Level (MSL)	MSL	3	Level

* Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to Absolute Maximum Rated conditions for extended periods may affect device reliability.

*Voltages are referenced to GND unless otherwise noted.

8 Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
VDD Input Voltage	VDD	3	3.3	5.5	V
VCONN Input Voltage	VCONN	3.3	5	5.5	V
VCONN Supply Current	I_{VCONN}	200		600	mA
Ambient Temperature	T_A	-40		85	℃

* Devices' performance cannot be guaranteed when working beyond those Recommended Operating Conditions.

9 Electrical Characteristics

Unless otherwise specified, TA=25℃, 3V ≤ VDD ≤ 5.5V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Consumption						
Shutdown Mode	$I_{shutdown}$	The CC pin exposes RD and disables all functions except I2C functions VDD = 3V to 5.5V VDD (Typ.) = 3.8V	20	25	43	uA
Low Power Mode	I_{LP_DRP}	CC toggle at DRP mode when port is unconnected and waiting for connection	25	30	50	uA

		VDD = 3V to 5.5V VDD (Typ.) = 3.8V				
Idle Mode	I_{iIdle_Sink}	Sink current consumption in cable attached with no PD communication VDD = 3V to 5.5V VDD (Typ.) = 3.8V	80	90	100	uA
Active Mode	I_{OP_Sink}	Sink current consumption in cable attached with PD transmitting continuous messages. VDD = 3V to 5.5V VDD (Typ.) = 3.8V	0.7	1.0	1.5	mA
VCONN						
Ron for VCONN Switch	R_{ON}	VCONN= 3V to 5.5V	--	0.7	1	Ω
VCONN OCP Setting Range	I_{OCP}	VDD = 3V to 5.5V, VCONN = 3.3V to 5.5V	200	--	600	mA
Threshold for detecting Vconn present	V_{VCONN_OK}	VDD = 3V to 5.5V,	2.2	--	2.5	V
Type-C						
DFP 80 µA CC Current	$DFP_{80\mu}$	VDD = 3V to 5.5V	64	80	96	uA
DFP 180 µA CC Current	$DFP_{180\mu}$	VDD = 3V to 5.5V	166	180	194	uA
DFP 330 µA CC Current	$DFP_{330\mu}$	VDD = 3V to 5.5V	304	330	356	uA
UFP Rd in Active Mode	Rd	VDD = 3V to 5.5V	4.6	5.1	5.6	kΩ
UFP Pull-Down Voltage in Dead Battery Under DFP80µA and DFP180 µA	V_{DBL}	VDD = 0V	--	--	1.6	V
UFP Pull-Down Voltage in Dead Battery Under DFP330 µA	V_{DBH}	VDD = 0V	--	--	2.6	V
PD BMC						
Bit Rate	$f_{BitRate}$	VDD = 3V to 5.5V	270	300	330	Kbps
Fall Time	t_{Fall}	VDD = 3V to 5.5V	300	--	--	ns
Rise Time	t_{Rise}	VDD = 3V to 5.5V	300	--	--	ns
Time from the end of last bit of a frame until the state of the first bit the next	$t_{Inter\ FrameCap}$	VDD = 3V to 5.5V	25	--	50	us

pre-amble						
Voltage Swing	V_{Swing}	VDD = 3V to 5.5V	1.050	1.125	1.200	V
Transmitter Output Impedance	z_{Driver}	VDD = 3V to 5.5V	33	--	75	Ω
Receiver Input Impedance	z_{BmcRx}	VDD = 3V to 5.5V	1	--	--	MΩ
I2C Electrical Characteristics						
SCL Clock Frequency	f_{OSCL}	VDD = 3V to 5.5V	0	--	3400	kHz
I2C Bus Supply Voltage	I2C_VDD	VDD = 3V to 5.5V	1.5	--	3.6	V
LOW-Level Input Voltage	V_{IL}	VDD = 3V to 5.5V	--	--	0.4	V
HIGH-Level Input Voltage	V_{IH}	VDD = 3V to 5.5V	1.3	--	--	V
LOW-Level Output Voltage	V_{OL}	VDD = 3V to 5.5V, Open-drain	--	--	0.4	V
Input Current Each IO Pin	I_I	VDD = 3V to 5.5V, $0.1V_{DD} < V_I < 0.9V_{DDMAX}$	-10	--	10	uA
Pulse width of spikes that must be suppressed by the input filter	t_{sp}	VDD = 3V to 5.5V	--	--	50	ns
Data Hold Time	$t_{HD:DAT}$	VDD = 3V to 5.5V	30	--	--	ns
Data Set-Up Time	$t_{SU:DAT}$	VDD = 3V to 5.5V	70	--	--	ns

10 Function Description

Shutdown mode

When powered on, IP2751 is in shutdown mode, in which only the I2C module and Rd works properly, and the power consumption of IC is about 25uA. In shutdown mode, if a register is set through the I2C module, the register value takes effect immediately but the corresponding function doesn't take effect. The corresponding function takes effect only after the system exit shutdown mode. IC exits shutdown mode when 0x9B[5] is set to 1.

Idle mode

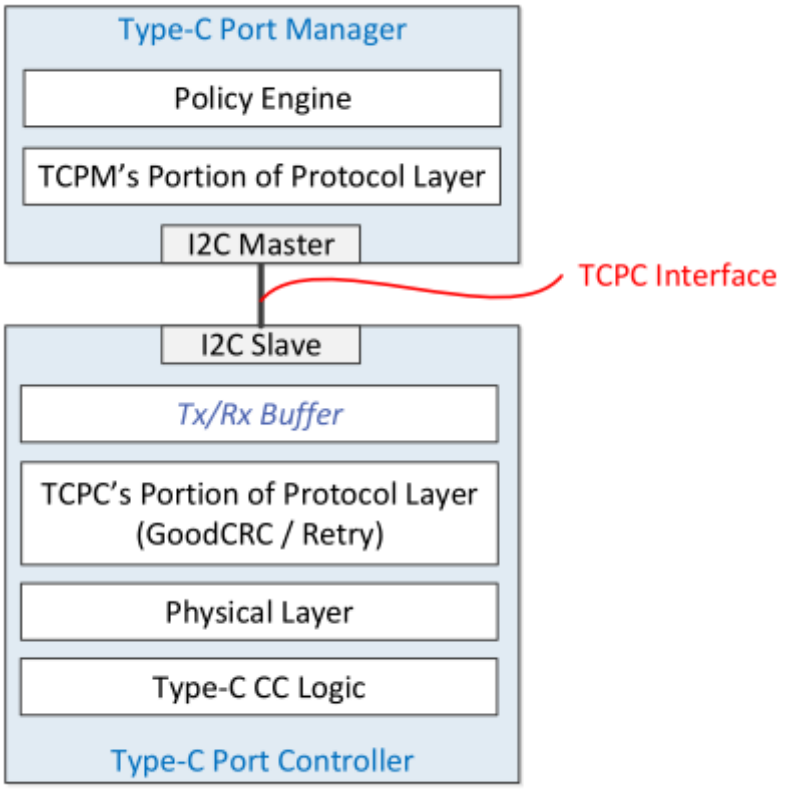
IP2751 enters automatic idle mode when 0x9B[3] is set to 1. When all INT are cleared and no interruption occurs, IC enters idle mode. In Idle mode, IC can still respond to interruption, and the power consumption is about 90uA. After the IC enters the idle mode, if an interruption occurs (INT_N is pulled down), the IC exits the idle mode and becomes active.

Low power mode

In non-shutdown mode, after 0x90[3] is set to 1, the system can directly enter the low power mode, start to sleep and wait for CC connection. After the system enters low power mode, if 0x9F[7] is set to 1, the system will wake up and exit low power mode when the CC connection is detected, and 0x90[3] will be cleared.

In low power mode, the power consumption of IC is about 30uA.

USB Type-C Port Controller (TCPC) Interface



The Type-C Port Controller Interface, TCPCI, is the interface between a Type-C Port Manager and a Type-C Port Controller.

The TCPC Interface uses the I2C protocol :

- The TCPM is the only master on this I2C bus
- The TCPC is a slave device on this I2C bus
- Each Type-C port has its own unique I2C slave address. The TCPC shall have equal numbers of unique I2C slave addresses and supported Type-C ports
- The TCPC supports Fast-mode bus speed
- The TCPC has an open drain active low output INT_N Pin. This pin is used to indicate change of state, where INT_N pin is asserted when any Alert Bits are set
- The TCPCI supports an I/O nominal voltage range of 1.8V to 3.3V
- The TCPC can auto-increment the I2C internal register of the last byte transferred during a read independent of an ACK/NACK from the master

Dead Battery Mode

IP2751 can support dead-battery mode by presenting Rd to both CC pins when VDD is no longer active. When exiting the dead battery mode, the RP/RD value is determined by the ROLE_CTL register (0x1A).

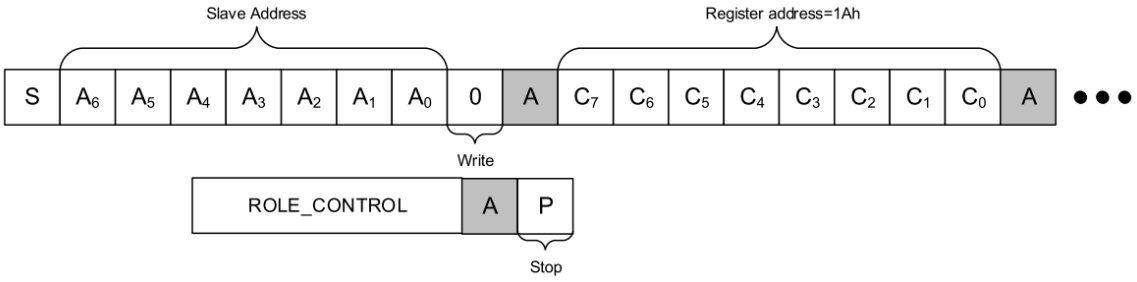
I2C

The default I2C address shows below

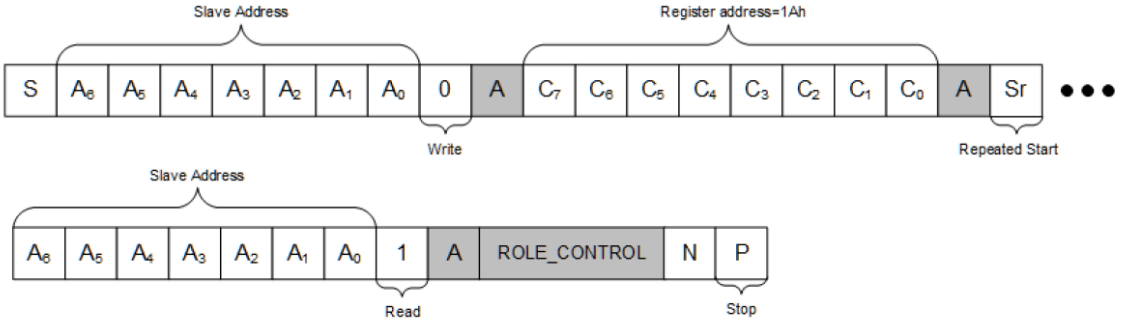
1	0	0	1	1	1	0	RW

MSB LSB

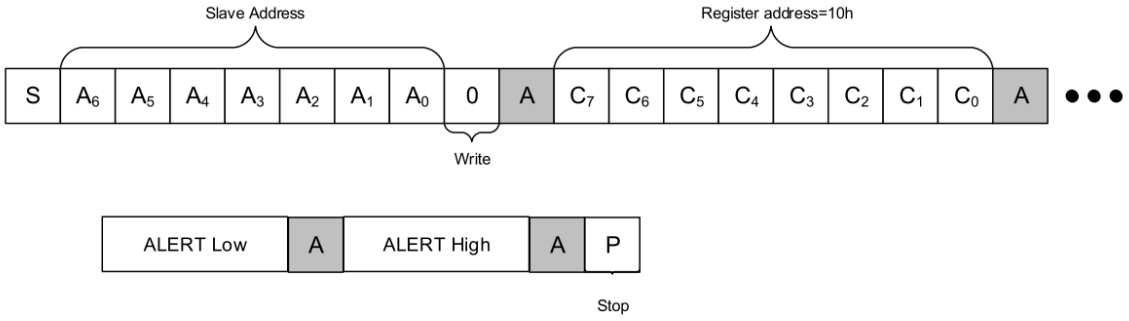
Writing Single Byte Registers:



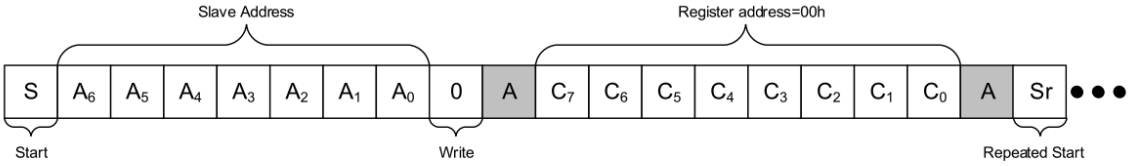
Reading Single Byte Registers:

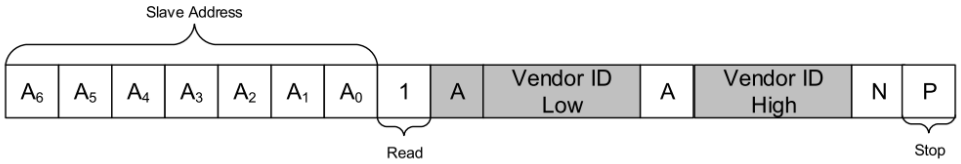


Writing Two-Byte Registers:

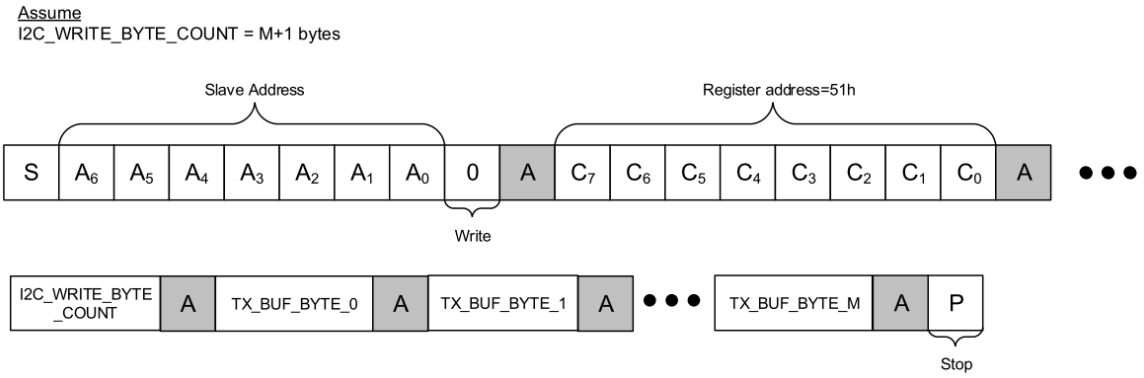


Reading Two-Byte Registers:

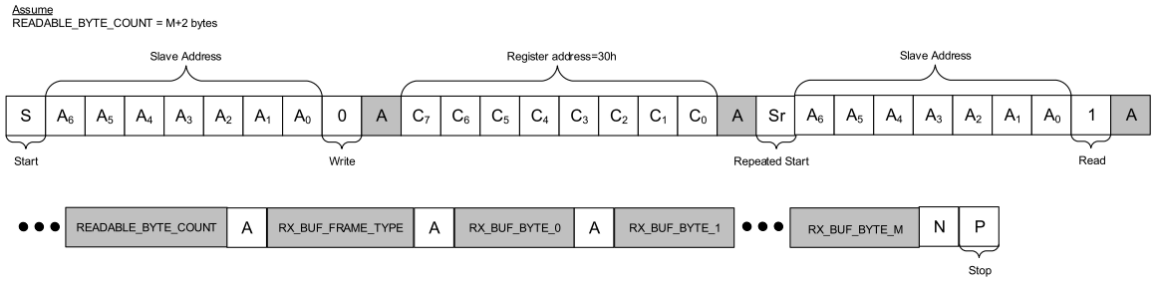




Writing the TRANSMIT_BUFFER:



Reading the RECEIVE_BUFFER:



TYPE-C

Two pins on the TypeC connector, CC1 and CC2 are used to establish and manage the Source-to-Sink connection.

Type-C source exposes independent pull-up(Rp) termination by current sources on CC1 and CC2 pins to advertise current capability and monitors the voltage by multiple comparators to detect a attach/detach.

Type-C sink exposes independent pull-down(Rd) terminations on CC1 and CC2 pins to detect current capability and monitors the voltage by multiple comparators to detect a attach/detach.

The TCPM may configure the TCPC to autonomously toggle the Rp/Rd when the TCPM-TCPC is implementing a DRP. When initiating autonomous DRP toggling, the TCPM shall write B6 (DRP) =1b and write the starting value of Rp/Rd to B3..0 (CC1/CC2) to indicate DRP autonomous toggling mode to the TCPC. The TCPC shall not start the DRP toggling until subsequently the TCPM writes to the COMMAND register to start the DRP toggling

PD Physical Layer

The USB PD Physical Layer consists of a pair of transmitters and receivers that communicate across a single signal wire (CC).

The transmitter performs the following functions:

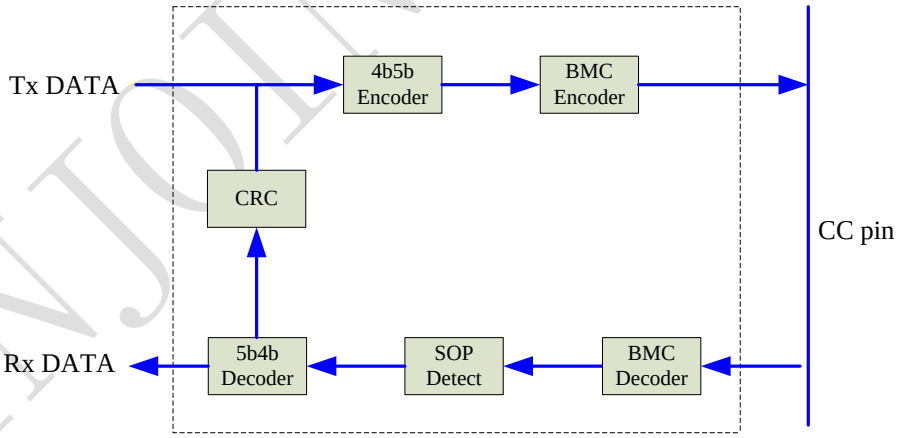
- Receive packet data from the protocol layer.
- Calculate and append a CRC.
- Encode the packet data including the CRC (i.e. the payload).
- Transmit the Packet (Preamble, SOP*, payload, CRC and EOP) across the channel using Biphase Mark Coding (BMC) over CC.

The receiver performs the following functions:

- Recover the clock and lock onto the Packet from the Preamble.
- Detect the SOP*.
- Decode the received data including the CRC.
- Detect the EOP and validate the CRC:

  If the CRC is Valid, deliver the packet data to the protocol layer.

  If the CRC is Invalid, flush the received data.



Transmitting PD Message

The steps for transmitting an SOP* USB PD message are as follows:

1. The TCPM writes the content of the message to be transmitted into the TRANSMIT_BUFFER
2. The TCPM writes to TRANSMIT requesting SOP* transmission.
3. The outcome of the write reported by the TCPC may be one of three indications after asserting the INT_N pin:

- If the TCPC PHY layer successfully transmits the message, the TCPC sets the Transmit SOP*Message Successful bit in the ALERT register.
- If the TCPC PHY layer did not get a response after retries, the TCPC sets the Transmit SOP*Message Failed bit in the ALERT register.
- If the transmission was discarded due to an incoming message, the TCPC sets the Transmit SOP*Message Discarded bit in the ALERT register.

4. Before requesting another transmission, the TCPM clears the alert by writing a logical 1 to the asserted bit in the ALERT register.

When transitioning through the steps of transmitting SOP* message, the TCPC may assert ALERT.Receive SOP*MessageStatus or ALERT.ReceivedHardReset bit at any time to notify that a message was received.

Receiving PD Message

The steps for receiving a short SOP* USB PD message are as follows:

1. The TCPC asserts the INT_N pin to request attention when it receives a Hard Reset, Cable Reset, or has sent the GoodCRC in response to an SOP* USB PD message from a Port Partner. If an overflow has occurred, the TCPC will have set the ALERT.RxBufferOverflow register, therefore the TCPC will not send the GoodCRC to other received messages until the TCPM clears the Message Received alert. The TCPM should always clear the Rx Buffer Overflow and Message Received bits at the same time. Otherwise there could be a scenario where the Rx Buffer Overflow bit remains set even though the TCPM has just cleared one of the messages in the buffer.
2. The TCPM reads the ALERT register and ALERT.ReceiveSOP*MessageStatus is asserted for notification that a message was received.
3. The TCPM reads the RECEIVE_BUFFER.READABLE_BYTE_COUNT and RECEIVE_BUFFER.RX_BUF_FRAME_TYPE. If the TCPC received an SOP* message, the TCPM reads as many bytes in the buffer (i.e. RECEIVE_BUFFER.RX_BUF_BYTE_x) as defined in the RECEIVE_BUFFER.READABLE_BYTE_COUNT. Note that RECEIVE_BUFFER.RX_BUF_FRAME_TYPE and RECEIVE_BUFFER.RX_BUF_BYTE_x are “hidden” and these registers can only be accessed by reading at address 30h .
4. The TCPM clears the Alerts:

   Writing ALERT.ReceiveSOP*MessageStatus to 1 also clears the receive buffer registers.
5. After the Alert and buffers have been cleared, the TCPC shall put the next received message (if any) into RECEIVE_BUFFER.RX_BUF_BYTE_x. The TCPC shall then update RECEIVE_BUFFER.READABLE_BYTE_COUNT and ALERT registers.

6. If INT_N pin is still asserted, return to Step 2.

11 Register Map

11.1 VENDOR_ID (00h...01h)

Bit(s)	Name	Description	R/W	Reset
15:0	VID[15:0]	A unique 16-bit unsigned integer. Assigned by the USB-IF to the Vendor.	0x2E87	R

11.2 PRODUCT_ID (02h...03h)

Bit(s)	Name	Description	R/W	Reset
15:0	PID[15:0]	A unique 16-bit unsigned integer.Assigned uniquely by the Vendor to identify the TCPC.	0x2751	R

11.3 DEVICE_ID (04h...05h)

Bit(s)	Name	Description	R/W	Reset
15:0	DID[15:0]	A unique 16-bit unsigned integer.Assigned uniquely by the Vendor to identify the TCPC.	0x0000	R

11.4 USBTYPEC_REV (06h...07h)

Bit(s)	Name	Description	R/W	Reset
15:0	USBTYPEC_REV	16-bit USB Type-C Revision. Revision	0x0011	R

11.5 USBPD_REV_VER (08h...09h)

Bit(s)	Name	Description	R/W	Reset
15:8	USBPD_REV	16-bit USB PD Revision. Revision	0x20	R
7:0	USBPD_VER	16-bit USB PD version. Version	0x11	R

11.6 PD_INTERFACE_REV (0Ah...0Bh)

Bit(s)	Name	Description	R/W	Reset
15:8	PDIF_REV	16-bit USB TCPC Revision. Revision	0x10	R
7:0	PDIF_VER	16-bit USB TCPC version. Version	0x10	R

11.7 ALERT (10h...11h)

Bit(s)	Name	Description	R/W	Reset
15	Reserved	Reserved	0	R
14	Reserved	Reserved	0	R
13	Reserved	Reserved	0	R
12	Reserved	Reserved	0	R
11	VBUS_SINK_DISCNT	Not support.	0	R
~~10~~	~~RXBUF_OVFLOW~~	~~0b : TCPC Rx buffer is functioning properly. (default)~~ ~~1b : TCPC Rx buffer has overflowed.~~	~~0~~	~~RW~~
9	FAULT	0b : No Fault. (default) 1b : A Fault has occurred. Read the FAULT_STATUS register.	0	RW
8	ALARM_VBUS_VOLTAGE_L	Not support.	0	R
7	ALARM_VBUS_VOLTAGE_H	Not support.	0	R
6	TX_SUCCESS	0b: Cleared (default) 1b : Reset or SOP* message transmission successful.	0	RW
5	TX_DISCARD	0b : Cleared (default) 1b : Reset or SOP* message transmission not sent due to incoming receive message.	0	RW
4	TX_FAIL	0b : Cleared (default) 1b : SOP* message transmission not successful, no GoodCRC response received on SOP* message transmission.	0	RW
3	RX_HARD_ RESET	0b : Cleared (default) 1b : Received Hard Reset message	0	RW

2	RX_SOP_MSG_STATUS	0b : Cleared (default) 1b : Receive status register changed	0	RW
1	POWER_STATUS	0b : Cleared 1b : Port status changed (default)	1	RW
0	CC_STATUS	0b : Cleared (default) 1b : CC status changed	0	RW

11.8 ALERT_MASK (12h...13h)

Bit(s)	Name	Description	R/W	Reset
15	Reserved	Reserved	0	R
14	Reserved	Reserved	0	R
13	Reserved	Reserved	0	R
12	Reserved	Reserved	0	R
11	M_VBUS_SINK_DISCNT	Not support.	1	R
~~10~~	~~M_RXBUF_OVFLOW~~	~~0b : Interrupt masked~~ ~~1b : Interrupt unmasked (default)~~	~~1~~	~~RW~~
9	M_FAULT	0b : Interrupt masked 1b : Interrupt unmasked (default)	1	RW
8	M_ALARM_VBUS_VOLTAGE_L	Not support.	1	R
7	M_ALARM_VBUS_VOLTAGE_H	Not support.	1	R
6	M_TX_SUCCESS	0b : Interrupt masked 1b : Interrupt unmasked (default)	1	RW
5	M_TX_DISCARD	0b : Interrupt masked 1b : Interrupt unmasked (default)	1	RW
4	M_TX_FAIL	0b : Interrupt masked 1b : Interrupt unmasked (default)	1	RW
3	M_RX_HARD_RESET	0b : Interrupt masked 1b : Interrupt unmasked (default)	1	RW
2	M_RX_SOP_MSG_STATUS	0b : Interrupt masked 1b : Interrupt unmasked (default)	1	RW
1	M_POWER_STATUS	0b : Interrupt masked 1b : Interrupt unmasked (default)	1	RW
0	M_CC_STATUS	0b : Interrupt masked	1	RW

		1b : Interrupt unmasked (default)		

11.9 POWER_STATUS_MASK (14h)

Bit(s)	Name	Description	R/W	Reset
7	Reserved	Not support.	1	R
~~6~~	~~M_TCPC_INITIAL~~	~~0b : Interrupt masked~~ ~~1b : Interrupt unmasked (default)~~	~~1~~	~~RW~~
5	M_SRC_HV	Not support.	1	RW
4	M_SRC_VBUS	Not support.	1	RW
3	M_VBUS_PRESENT_DETC	0b : Interrupt masked 1b : Interrupt unmasked (default)	1	RW
2	M_VBUS_PRESENT	0b : Interrupt masked 1b : Interrupt unmasked (default)	1	RW
1	M_VCONN_PRESENT	0b : Interrupt masked 1b : Interrupt unmasked (default)	1	RW
0	M_SINK_VBUS	Not support.	1	RW

11.10 FAULT_STATUS_MASK (15h)

Bit(s)	Name	Description	R/W	Reset
7	M_VCON_OV	0b : Interrupt masked (default) 1b : Interrupt unmasked	0	RW
6	M_FORCE_OFF_VBUS	0b : Interrupt masked 1b : Interrupt unmasked (default)	1	RW
5	M_AUTO_DISC_FAIL	0b : Interrupt masked 1b : Interrupt unmasked (default)	1	RW
4	M_FORCE_DISC_FAIL	0b : Interrupt masked 1b : Interrupt unmasked (default)	1	RW
3	M_VBUS_OC	0b : Interrupt masked 1b : Interrupt unmasked (default)	1	RW
2	M_VBUS_OV	0b : Interrupt masked 1b : Interrupt unmasked (default)	1	RW
1	M_VCON_OC	0b : Interrupt masked	1	RW

		1b : Interrupt unmasked (default)		
0	M_I2C_ERROR	0b : Interrupt masked 1b : Interrupt unmasked (default)	1	RW

11.11 CONFIG_STANDARD_OUTPUT (18h)

Bit(s)	Name	Description	R/W	Reset
7	H_IMPEDENCE	Not support.	0	R
6	DBG_ACC_CONNECT_O	Not support.	0	R
5	AUDIO_ACC_CONNECT	Not support.	0	R
4	ACTIVE_CABLE_CONNECT	Not support.	0	R
3:2	MUX_CTRL	Not support.	00	R
1	CONNECT_PRESENT	Not support.	0	R
0	CONNECT_ORIENT	Not support.	0	R

11.12 TCPC_CTL (19h)

Bit(s)	Name	Description	R/W	Reset
7:5	Reserved	Reserved	000	R
4	Reserved	Reserved	0	R
3:2	I2C_CK_STRETCH	Not support.	00	R
~~1~~	~~BIST_TEST_MODE~~	~~0b : Normal Operation. Incoming messages enabled by RECEIVE_DETECT passed to TCPM via Alert. (default)~~ ~~1b : BIST Test Mode. Incoming messages enabled by RECEIVE_DETECT result in GoodCRC response but may not be passed to the TCPM via Alert. TCPC may temporarily store incoming messages in the Receive Message Buffer, but this may or may not result in a Receive SOP* Message Status or a Rx Buffer Overflow alert.~~	~~0~~	~~RW~~
0	PLUG_ORIENT	0b : When VCONN is enabled, apply it to the CC2 pin. Monitor the CC1 pin for BMC communications if PD messaging is enabled. (default)	0	RW

		1b : When VCONN is enabled, apply it to the CC1 pin. Monitor the CC2 pin for BMC communications if PD messaging is enabled. Required		

11.13 ROLE_CTL (1Ah)

Bit(s)	Name	Description	R/W	Reset
7	Reserved	Reserved	0	R
6	DRP	0b : No DRP. Bits B3..0 determine Rp/Rd/Ra settings (default) 1b: DRP	0	RW
5:4	RP_VALUE	00b : Rp default (default) 01b : Rp 1.5A 10b : Rp 3.0A 11b : Reserved	00	RW
3:2	CC2	00b : Reserved 01b : Rp (Use Rp definition in B5..4) 10b : Rd (default) 11b : Open (Disconnect or don't care) Set to 11b if enabling DRP in B7..6	10	RW
1:0	CC1	00b : Reserved 01b : Rp (Use Rp definition in B5..4) 10b : Rd (default) 11b : Open (Disconnect or don't care) Set to 11b if enabling DRP in B7..6	10	RW

11.14 FAULT_CTL (1Bh)

Bit(s)	Name	Description	R/W	Reset
7	DIS_VCON_OV	0b : Fault detection circuit enabled (default) 1b : Fault detection circuit disabled	0	RW
6:5	Reserved	Reserved	00	R
4	DIS_FORCE_OFF_VBUS	Not support.	0	R

3	DIS_VBUS_DISC_FAULT_TIMER	Not support.	0	R
2	DIS_VBUS_OC	Not support.	0	R
1	DIS_VBUS_OV	Not support.	0	R
0	DIS_VCON_OC	0b : Fault detection circuit enabled (default) 1b : Fault detection circuit disabled	0	RW

11.15 POWER_CTL (1Ch)

Bit(s)	Name	Description	R/W	Reset
7	Reserved	Reserved	0	R
6	VBUS_VOL_MONITOR	Not support.	0	R
5	DIS_VOL_ALARM	Not support.	0	R
4	AUTO_DISC_DISCNCT	Not support.	0	R
3	BLEED_DISC	Not support.	0	R
2	FORCE_DISC	Not support.	0	R
1	VCONN_POWER_SPT	0b : TCPC delivers at least 1W on VCONN (default) 1b : TCPC delivers at least the power indicated in DEVICE_CAPABILITIES. VCONNPowerSupported	0	RW
0	EN_VCONN	0b : Disable VCONN Source (default) 1b : Enable VCONN Source to CC Required	0	RW

11.16 CC_STATUS (1Dh)

Bit(s)	Name	Description	R/W	Reset
7:6	Reserved	Reserved	00	R
5	DRP_STATUS	0b : the TCPC has stopped toggling or (ROLE_CONTROL.DRP = 00) (default) 1b : the TCPC is toggling	0	R
4	DRP_RESULT	0b : the TCPC is presenting Rp (default) 1b : the TCPC is presenting Rd	0	R

3:2	CC2_STATUS	If (ROLE_CONTROL.CC2 = Rp) or
		(DrpResult = 0)
		00b : SRC.Open (Open, Rp) (default)
		01b : SRC.Ra (below maximum vRa)
		10b : SRC.Rd (within the vRd range)
		11b : reserved
		
		If (ROLE_CONTROL.CC2 = Rd) or
		(DrpResult = 1)
		00b: SNK.Open (Below maximum vRa) (default)
		01b: SNK.Default (Above minimum vRd-Connect)
		10b: SNK.Power1.5 (Above minimum vRd-Connect) Detects Rp 1.5A
		11b: SNK.Power3.0 (Above minimum vRd-Connect) Detects Rp 3.0A
		
		If ROLE_CONTROL.CC2 = Ra, this field is set to 00b
		If ROLE_CONTROL.CC2 = Open, this field is set to 00b
		
		This field always returns 00b if (DrpStatus = 1) or (POWER_CONTROL.EnableVCONN =
		1 and POWER_CONTROL.PlugOrientation = 0). Otherwise, the returned value depends upon ROLE_CONTROL.CC2.
			00	R

1:0	CC1_STATUS	If (ROLE_CONTROL.CC1 = Rp) or
		(DrpResult = 0)
		00b : SRC.Open (Open, Rp) (default)
		01b : SRC.Ra (below maximum vRa)
		10b : SRC.Rd (within the vRd range)
		11b : reserved
		
		If (ROLE_CONTROL.CC1 = Rd) or
		DrpResult = 1)
		00b : SNK.Open (Below maximum
		vRa) (default)
			00	R

		01b: SNK.Default (Above minimum vRd-Connect) 10b : SNK.Power1.5 (Above minimum vRd-Connect) Detects Rp-1.5A 11b : SNK.Power3.0 (Above minimum vRd-Connect) Detects Rp-3.0A If ROLE_CONTROL.CC1 = Ra, this field is set to 00b If ROLE_CONTROL.CC1 = Open, this field is set to 00b This field always returns 00b if (DrpStatus = 1) or (POWER_CONTROL.EnableVCONN = 1 and POWER_CONTROL.PlugOrientation = 0). Otherwise, the returned value depends upon ROLE_CONTROL.CC1.		

11.17 POWER_STATUS (1Eh)

Bit(s)	Name	Description	R/W	Reset
7	DBG_ACC_CONNECT	Not support.	0	R
~~6~~	~~TCPC_INITIAL~~	~~0b : The TCPC has completed initialization and all registers are valid (default)~~ ~~1b : The TCPC is still performing internal initialization and the only registers that are guaranteed to return the correct values are 00h..0Fh~~	~~0~~	~~R~~
5	SRC_HV	Not support.	0	R
4	SRC_VBUS	Not support.	0	R
3	VBUS_PRESENT_DETC	0b : VBUS present detection disabled 1b : VBUS present detection enabled (default)	1	R
2	VBUS_PRESENT	0b : VBUS Disconnected (default) 1b : VBUS Connected	0	R
1	VCONN_PRESENT	0b : VCONN is not present (default) 1b : This bit is asserted when VCONN present CC1 or CC2. Threshold is fixed at 2.4V	0	R
0	SINK_VBUS	Not support.	0	R

11.18 FAULT_STATUS (1Fh)

Bit(s)	Name	Description	R/W	Reset
7	VCON_OV	0b : Not in an over-voltage protection state (default) 1b : Over-voltage fault latched.	0	RW
6	FORCE_OFF_VBUS	Not support.	0	R
5	AUTO_DISC_FAIL	Not support.	0	R
4	FORCE_DISC_FAIL	Not support.	0	R
3	VBUS_OC	Not support.	0	R
2	VBUS_OV	Not support.	0	R
1	VCON_OC	0b : No fault detected (default) 1b : Over-current VCONN fault latched	0	RW
0	I2C_ERROR	Not support.	0	R

11.19 COMMAND (23h)

Bit(s)	Name	Description	R/W	Reset
7:0	COMMAND	0010 0010b : DisableVbusDetect: Disable Vbus present and vSafe0V detection. 0011 0011b : EnableVbusDetect: Enable Vbus present and vSafe0V detection. 1001 1001b : Start DRP Toggling if ROLE_CONTROL.DRP = 1b. If ROLE_CONTROL.CC1/CC2= 01b start with Rp, if ROLE_CONTROL.CC1/CC2 =10b start with Rd.	0x00	RW

11.20 DEVICE_CAPABILITIES_1 (24h...25h)

Bit(s)	Name	Description	R/W	Reset
15	Reserved	Reserved	0	R
14	CPB_VBUS_OC	0b : VBUS OCP is not reported by the TCPC (default) 1b : VBUS OCP is reported by the TCPC	0	R
13	CPB_VBUS_OV	0b : VBUS OVP is not reported by the TCPC	0	R

		(default) 1b : VBUS OVP is reported by the TCPC		
12	CPB_BLEED_DISC	0b : No Bleed Discharge implemented in TCPC (default) 1b : Bleed Discharge is implemented in the TCPC	0	R
11	CPB_FORCE_DISC	0b : No Force Discharge implemented in TCPC (default) 1b : Force Discharge is implemented in the TCPC	0	R
10	VBUS_MEASURE_ALARM	0b : No VBUS voltage measurement nor VBUS Alarms (default) 1b : VBUS voltage measurement and VBUS Alarms	0	R
9:8	SOURCE_RP_SUPPORT	00b : Rp default only 01b : Rp 1.5A and default 10b : Rp 3.0A, 1.5A, and default (default) 11b : Reserved Rp values which may be configured by the TCPM via the ROLE_CONTROL register	10	R
7:5	ROLES_SUPPORT	000b : Type-C Port Manager can configure the Port as Source only or Sink only (not DRP) 001b : Source only 010b : Sink only 011b : Sink with accessory support (optional) 100b : DRP only 101b : Adapter or Cable (Ra) only 110b : Source, Sink, DRP, Adapter/Cable all supported (default) 111b : Not valid	110	R
4	ALL_SOP_SUPPORT	0b : All SOP* except SOP'_DBG/SOP"_DBG 1b : All SOP* messages are supported (default)	1	R
3	SOURCE_VCONN	0b : TCPC is not capable of switching VCONN 1b : TCPC is capable of switching VCONN (default)	1	R
2	CPB_SINK_VBUS	0b : TCPC is not capable controlling the sink path to the system load (default)	0	R

		1b : TCPC is capable of controlling the sink path to the system load		
1	SOURCE_HV_VBUS	0b : TCPC is not capable of controlling the source high voltage path to VBUS (default) 1b : TCPC is capable of controlling the source high voltage path to VBUS	0	R
0	SOURCE_VBUS	0b : TCPC is not capable of controlling the source path to VBUS (default) 1b : TCPC is capable of controlling the source path to VBUS	0	R

11.21 DEVICE_CAPABILITIES_2 (26h...27h)

Bit(s)	Name	Description	R/W	Reset
15:8	Reserved	Reserved	0x00	R
7	SINK_DISCONNECT_DET	0b : VBUS_SINK_DISCONNECT_THRESH OLD not implemented (default: Use POWER_STATUS.VbusPresent = 0b to indicate a Sink disconnect) (default) 1b : VBUS_SINK_DISCONNECT_THRESH OLD implemented	0	R
6	STOP_DISC_THD	0b : VBUS_STOP_DISCHARGE_THRESH OLD not implemented (default) 1b : VBUS_STOP_DISCHARGE_THRESH OLD implemented	0	R
5:4	VBUS_VOL_ALARM_LSB	00b : TCPC has 25mV LSB for its voltage alarm and uses all 10 bits in VBUS_VOLTAGE_ALARM_HI_CFG and VBUS_VOLTAGE_ALARM_LO_CFG. 01b : TCPC has 50mV LSB for its voltage alarm and uses only 9 bits. VBUS_VOLTAGE_ALARM_HI_CFG[0] and	11	R

		VBUS_VOLTAGE_ALARM_LO_CFG[0] are ignored by TCPC. 10b : TCPC has 100mV LSB for its voltage alarm and uses only 8 bits. VBUS_VOLTAGE_ALARM_HI_CFG[1:0] and VBUS_VOLTAGE_ALARM_LO_CFG[1:0] are ignored by TCPC. 11b : Not support this function. (default)		
3	VCONN_POWER	000b : 1.0W 001b : 1.5W 010b : 2.0W (default) 011b : 3W 100b : 4W 101b : 5W 110b : 6W 111b : External	010	R
0	VCONN_OCF	0b : TCPC is not capable of detecting a VCONN fault 1b : TCPC is capable of detecting a VCONN fault (default)	1	R

11.22 STANDARD_INPUT_CAPABILITIES (28h)

Bit(s)	Name	Description	R/W	Reset
7:3	Reserved	Reserved	0000	R
2	VBUS_EXT_OVF	0b : Not present in TCPC (default) 1b : Present in TCPC.	0	R
1	VBUS_EXT_OCF	0b : Not present in TCPC (default) 1b : Present in TCPC	0	R
0	FORCE_OFF_VBUS_IN	0b : Not present in TCPC (default) 1b : Present in TCPC	0	R

11.23 STANDARD_OUTPUT_CAPABILITIES (29h)

Bit(s)	Name	Description	R/W	Reset

7	Reserved	Reserved	0	R
6	CPB_DBG_ACC_IND	0b : Not present in TCPC (default) 1b : Present in TCPC	0	R
5	CPB_VBUS_PRESENT_MNT	0b : Not present in TCPC (default) 1b : Present in TCPC	0	R
4	CPB_AUDIO_ADT_ACC_IND	0b : Not present in TCPC (default) 1b : Present in TCPC	0	R
3	CPB_ACTIVE_CABLE_IND	0b : Not present in TCPC (default) 1b : Present in TCPC	0	R
2	CPB_MUX_CFG_CTRL	0b : Not present in TCPC (default) 1b : Present in TCPC	0	R
1	CPB_CONNECT_PRESENT	0b : Not present in TCPC (default) 1b : Present in TCPC	0	R
0	CPB_CONNECT_ORIENT	0b : Not present in TCPC (default) 1b : Present in TCPC	0	R

11.24 MESSAGE_HEADER_INFO (2Eh)

Bit(s)	Name	Description	R/W	Reset
7:5	Reserved	Reserved	000	R
4	CABLE_PLUG	0b : Message originated from Source, Sink, or DRP (default) 1b : Message originated from a Cable Plug	0	RW
3	DATA_ROLE	0b : Sink (default) 1b : Source	0	RW
2:1	USBPD_SPECREV	00b : Revision 1.0 01b : Revision 2.0 (default) 10b : Revision 3.0 11b : Reserved	01	RW
0	POWER_ROLE	0b : Sink (default) 1b : Source	0	RW

11.25 RECEIVE_DETECT (2Fh)

Bit(s)	Name	Description	R/W	Reset
7	Reserved	Reserved	0	R
6	EN_CABLE_RST	0b: TCPC does not detect Cable Reset signaling (default) 1b : TCPC detects Cable Reset signaling	0	RW
5	EN_HARD_RST	0b: TCPC does not detect Hard Reset signaling (default) 1b : TCPC detects Hard Reset signaling	0	RW
4	EN_SOP2DB	0b: TCPC does not detect SOP_DBG'' message (default) 1b : TCPC detects SOP_DBG'' message	0	RW
3	EN_SOP1DB	0b : TCPC does not detect SOP_DBG' message (default) 1b : TCPC detects SOP_DBG' message	0	RW
2	EN_SOP2	0b : TCPC does not detect SOP'' message (default) 1b : TCPC detects SOP'' message	0	RW
1	EN_SOP1	0b : TCPC does not detect SOP' message (default) 1b : TCPC detects SOP' message	0	RW
0	EN_SOP	0b : TCPC does not detect SOP message (default) 1b : TCPC detects SOP message	0	RW

11.26 RECEIVE_BUFFER (30h~4Fh)

READABLE_BYTE_COUNT(30h)

Bit(s)	Name	Description	R/W	Reset
7:0	RX_BYTE_COUNT	Indicates number of bytes in this register that are not stale. The TCPM should read the first RECEIVE_BYTE_COUNT bytes in this register.	0x00	RW

RX_BUF_FRAME_TYPE(31h)

Bit(s)	Name	Description	R/W	Reset
7:3	Reserved	Reserved	0000	R
2:0	RX_FRAME_TYPE	Type of received frame 000b : Received SOP (default) 001b : Received SOP' 010b : Received SOP'' 011b : Received SOP_DBG' 100b : Received SOP_DBG'' 110b : Received Cable Reset All others are reserved.	000	R

RX_BUF_BYTE_x(32h~4Fh)

Bit(s)	Name	Description	R/W	Reset
7:0	RX_BUF_BYTE_x	Receive Buffer Bytes. These registers are "hidden" and can only be accessed by reading at address 30h.	0x00	RW

11.27 TRANSMIT (50h)

Bit(s)	Name	Description	R/W	Reset
7:6	Reserved	Reserved	00	R
5:4	TX_RETRY_CNT	00b : No message retry is required (default) 01b : Automatically retry message transmission once 10b : Automatically retry message transmission twice 11b : Automatically retry message transmission three times	0	RW
3	Reserved	Reserved	0	R
2:0	TX_FRAME_TYPE	000b : Transmit SOP (default) 001b : Transmit SOP' 010b : Transmit SOP'' 011b : Transmit SOP_DBG'	000	RW

		100b : Transmit SOP_DBG'' 101b : Transmit Hard Reset 110b : Transmit Cable Reset 111b : Transmit BIST Carrier Mode 2 (TCPC shall exit the BIST mode no later than tBISTContMode max)		

11.28 TRANSMIT_BUFFER (51h~6Fh)

I2C_WRITE_BYTE_COUNT(51h)

Bit(s)	Name	Description	R/W	Reset
7:0	I2C_WRITE_BYTE_COUNT	The number of bytes the TCPM intends to write to the TX_BUF_BYTE_x in the given I2C/SMBus transaction. The TCPM shall write as many bytes in the buffer as defined in this register in one I2C write transaction. If DEVICE_CAPABILITIES_2.LongMessage = 0, the TCPC shall ignore the I2C transaction if I2C_WRITE_BYTE_COUNT is more than 30. If DEVICE_CAPABILITIES_2.LongMessage = 1, the TCPC shall ignore the I2C transaction if I2C_WRITE_BYTE_COUNT is more than 132.	0x00	RW

TX_BUF_BYTE_x(52h~6Fh)

Bit(s)	Name	Description	R/W	Reset
7:0	TX_BUF_BYTE_x	Transmit Buffer Bytes. These registers are "hidden" and can only be accessed by writing to address 51h.	0x00	RW

11.29 USER_CTL0(90h)

Bit(s)	Name	Description	R/W	Reset
7	Reserved	Reserved	0	R

6	Reserved	Reserved	0	RW
5	VCONN DISCHARGE_EN	VCONN OVP occurs and discharge path turn-on 0b : No discharge (default) 1b : Discharge	0	RW
4	LPRPRD	Low power mode Rp/Rd enable 0b : Low power mode RD (default) 1b : Low power mode RP	0	RW
3	LPEN	Low power mode enable 0b : Idle mode (default) 1b : Low power	0	RW
2	BG_EN	BMCIO BandGap enable 0b : BandGap off CC pin function disable 1b : BandGap on (default) CC pin function enable	1	RW
1	VBUS_DETEN	VBUS detection enable 0b : Measure off 1b : Operation (default)	1	RW
0	OSC_EN	24M oscillator for BMC communication 0b : Disable 24M oscillator 1b : Enable 24M oscillator (default) Note : 24M oscillator will be enabled automatically when INT occur.	1	RW

11.30 USER_CTL1(93h)

Bit(s)	Name	Description	R/W	Reset
7:5	VCONOCP[2:0]	VCONN over-current control selection 000b : Current level = 200mA 001b : Current level = 300mA 010b : Current level = 400mA 011b : Current level = 500mA 100b : Current level = 600mA	100	RW

		(default) 101 to 111b : Reserved		
4:1	Reserved	Reserved	0000	R
0	Reserved	Reserved	1	RW

11.31 USER_STATUS(97h)

Bit(s)	Name	Description	R/W	Reset
7	CC2OV	0b : CC2 not over voltage 1b : CC2 over voltage	0	R
6	CC1OV	0b : CC1 not over voltage 1b : CC1 over voltage	0	R
5:2	Reserved	Reserved	0	R
1	VBUS_0P80	0b : VBUS over 0.8V (default) 1b : VBUS under 0.8V	0	R
0	Reserved	Reserved	0	R

11.32 USER_INT(98h)

Bit(s)	Name	Description	R/W	Reset
7	INT_CC2OV	0b : Cleared (default) 1b : CC2 OV	0	R
6	INT_CC1OV	0b : Cleared (default) 1b : CC1 OV	0	R
5	INT_RA_DETACH	0b : Cleared (default) 1b : Ra detach	0	RW
4:2	Reserved	Reserved	000	RW
1	INT_VBUS_80	0b : VBUS without under 0.8V (default) 1b : VBUS under 0.8V	0	RW
0	INT_WAKEUP	0b : Cleared (default) 1b : Low power mode exited	0	RW

11.33 USER_MASK(99h)

Bit(s)	Name	Description	R/W	Reset
7	M_CC2OV	0b : Interrupt masked (default) 1b : Interrupt unmasked	0	R
6	M_CC1OV	0b : Interrupt masked (default) 1b : Interrupt unmasked	0	R
5	M_RA_DETACH	0b : Interrupt masked (default) 1b : Interrupt unmasked	0	RW
4:2	Reserved	Reserved	000	RW
1	M_VBUS_80	0b : Interrupt masked (default) 1b : Interrupt unmasked	0	RW
0	M_WAKEUP	0b : Interrupt masked (default) 1b : Interrupt unmasked	0	RW

11.34 USER_CTL2(9Bh)

Bit(s)	Name	Description	R/W	Reset
7	Reserved	Reserved	1	R
6	Reserved	Reserved	0	R
5	Shutdown_OFF	0 : Shutdown mode (default) 1 : Non-Shutdown mode	0	RW
4	Reserved	Reserved	0	R
3	AUTOIDLE_EN	1 : Auto enter idle mode enable (default) 0 : Auto enter idle mode disable	0	RW
2:0	AUTOIDLE_TIMEOUT	Enter idle mode timeout time =(AUTOIDLE_TIMEOUT*2+1)*6.4ms	000	RW

11.35 USER_CTL3(9Fh)

Bit(s)	Name	Description	R/W	Reset
7	WAKEUP_EN	0 : Wakeup function disable 1 : Wakeup function enable (default)	1	RW
6:4	Reserved	Reserved	000	R
3:2	Reserved	Reserved	00	RW
1	CC2OV_EN	CC2 OV enable: 0 : CC OV function disable(default) 1 : CC OV function enable	00	RW
0	CC1OV_EN	CC1 OV enable: 0 : CC OV function disable(default) 1 : CC OV function enable	00	RW

11.36 USER_RESET(A0h)

Bit(s)	Name	Description	R/W	Reset
7:1	Reserved	Reserved	0000000	R
0	SOFT_RESET	Write 1 to trigger software reset.	0	W

11.37 USER_tDRP(A2h)

Bit(s)	Name	Description	R/W	Reset
7:4	Reserved		0000	R
3:0	TDRP	The period a DRP will complete a Source to Sink and back advertisement. (Period = TDRP*6.4+51.2ms) 0000 : 51.2ms 0001 : 57.6ms 0010 : 64ms 0011 : 70.4ms (default) …	0011	RW

		1110 : 140.8ms 1111 : 147.2ms		

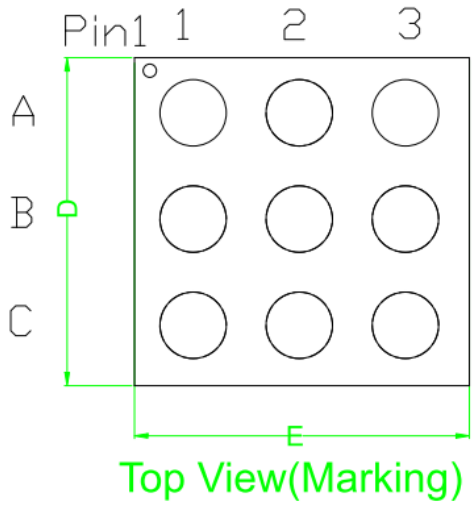
11.38 USER_DUTY0(A3h)

Bit(s)	Name	Description	R/W	Reset
7:0	DCSRCDRP[7:0]	The percent of time that a DRP will advertise Source during tDRP. (DUTY=(DCSRCDRP[9:0]+1)/1024) 0000000000 : 1/1024 0000000001 : 2/1024 … 0101000111 : 328/1024 (default) … 1111111110 : 1023/1024 1111111111 : 1024/1024 Note : Setting with 0xA4[9:8]	01000111	RW

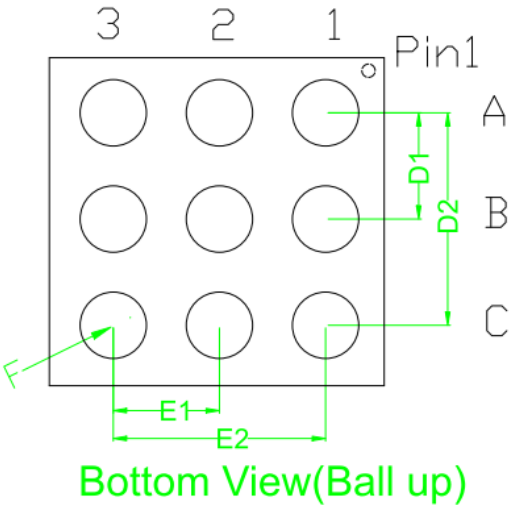
11.39 USER_DUTY1(A4h)

Bit(s)	Name	Description	R/W	Reset
7:2	Reserved		000000	R
1:0	DCSRCDRP[9:8]	The percent of time that a DRP will advertise Source during tDRP. (DUTY=(DCSRCDRP[9:0]+1)/1024) 0000000000 : 1/1024 0000000001 : 2/1024 … 0101000111 : 328/1024 (default) … 1111111110 : 1023/1024 1111111111 : 1024/1024 Note : Setting with 0xA4[9:8]	01	RW

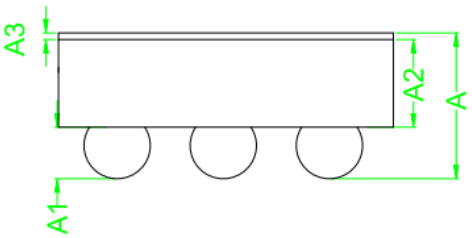
12 Package



Top View(Marking)



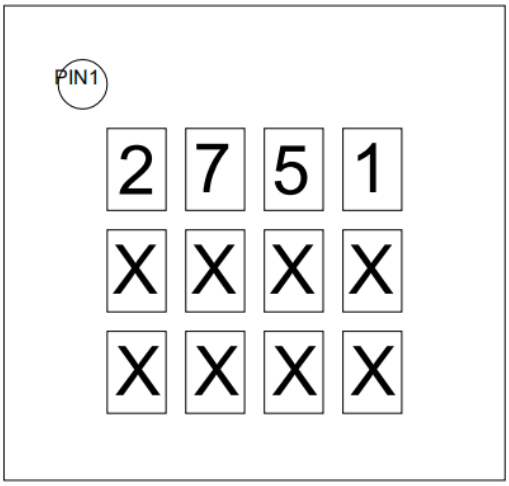
Bottom View(Ball up)



Item		No.	Mean/mm	Tolerance
总厚度		A	0.549	±0.0375
球高		A1	0.194	±0.020
Wafer Thickness		A2	0.330	±0.0125
背胶厚度		A3	0.025	±0.005
芯片尺寸	X	E	1.257	±0.025
	Y	D	1.230	±0.025
球尺寸		F	0.268	±0.020
球间距		D1	0.400	NA
		E1	0.400	NA
		D2	0.800	NA
		E2	0.800	NA

13 Marking Specification

The top pictures of IP2751 are shown as below:



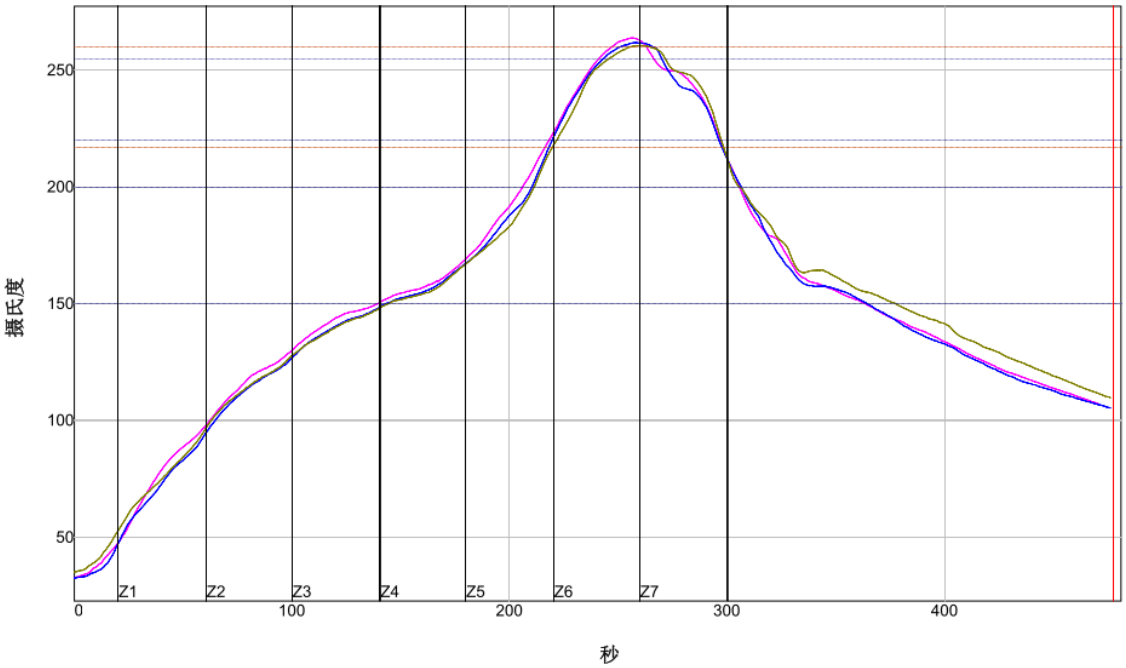
说明：

1：2751 ——代表产品型号IP2751

2：XXXX
XXXX ——生产批号

14 Solder Instruction

温度设置 (摄氏度)							
温区	1	2	3	4	5	6	7
上温区	130	140	160	160	200	320	265
下温区	130	140	160	160	200	320	265
传送带速度 (公分/分):	39.0						



PWI= 75%	最高上升斜率		预热150至200C		最高温度		总共 时间 /217C		斜率1 (217-260C)		预热220至255C-(2)		总共 时间 /260C-2		距峰值5C区域时间	
VP 1	1.69	-31%	66.21	-59%	263.87	18%	80.99	-70%	1.70	-30%	22.81	-36%	15.90	-30%	18.13	-75%
VP 2	1.99	-1%	66.91	-54%	261.84	-9%	78.97	-73%	1.87	-13%	23.44	-33%	15.74	-31%	23.64	-31%
VP 3	1.83	-17%	66.61	-56%	260.76	-23%	78.19	-74%	1.88	-12%	23.97	-30%	9.37	-66%	23.95	-28%
温差	0.30		0.70		3.11		2.80		0.18		1.16		6.53		5.82	

制程界限:

锡膏:	260		
统计数名称	最低界限	最高界限	单位
最高温度上升斜率 (目标=2.0) (计算斜率的时间距离= 20 秒)	1.0	3.0	度/秒
斜率1 (目标=2.0) 介于 217.0 和 260.0 (计算斜率的时间距离= 10 秒)	1.0	3.0	度/秒
预热时间150-200摄氏度	60	90	秒
预热时间220-255摄氏度-(2)	10	50	秒
最高温度	255	270	度 摄氏度
在217摄氏度以上时间	60	200	秒
在260摄氏度以上时间-(2)	3	40	秒
距峰值5C区域时间	15	40	秒

15 IMPORTANT NOTICE

INJOINIC TECHNOLOGY and its subsidiaries reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to INJOINIC TECHNOLOGY's terms and conditions of sale supplied at the time of order acknowledgment.

INJOINIC TECHNOLOGY assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using INJOINIC TECHNOLOGY's components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of INJOINIC TECHNOLOGY's components in its applications, notwithstanding any applications-related information or support that may be provided by INJOINIC TECHNOLOGY. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify INJOINIC TECHNOLOGY and its representatives against any damages arising out of the use of any INJOINIC TECHNOLOGY's components in safety-critical applications.

Reproduction of significant portions of INJOINIC TECHNOLOGY's information in INJOINIC TECHNOLOGY's data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. INJOINIC TECHNOLOGY is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

INJOINIC TECHNOLOGY will update this document from time to time. The actual parameters of the product may vary due to different models or other items. This document voids all express and any implied warranties.

Resale of INJOINIC TECHNOLOGY's components or services with statements different from or beyond the parameters stated by INJOINIC TECHNOLOGY for that component or service voids all express and any implied warranties for the associated INJOINIC TECHNOLOGY's component or service and is an unfair and deceptive business practice. INJOINIC TECHNOLOGY is not responsible or liable for any such statements.

