JW7953

20W/20V Full-Bridge with Demodulation and LDO for the Wireless Charger Transmitter

Preliminary Specifications Subject to Change without Notice

DESCRIPTION

The JW7953 is a high efficiency full-bridge power stage with voltage/current demodulation designed for wireless charger transmitter. With a transmitter controller, it can provide flexible wireless charger solutions compliant with Qi v2.0 Baseline Power Profile (BPP), Extended Power Profile (EPP) and Magnetic Power Profile (MPP).

The JW7953 integrates a 4-MOSFETs full-bridge with low $R_{DS(ON)}$, gate drivers, 5V LDO, 3.3V LDO, input current sensor, voltage/current communication demodulation, Q factor detection, resonant capacitor switching drivers and protection circuits.

The JW7953 provides input current sense function. The chip measures the input current with the current sampling resistor and reports it on the CSO pin, so that the transferred power can be detected by the controller. The controller realizes foreign object detection (FOD) by continuously monitoring transferred power and received power. For EPP/MPP equipment, Q factor detection is required to realize foreign object protection by comparing with the set Q threshold.

The JW7953 guarantees robustness with under-voltage lockout (UVLO), input over-voltage protection (OVP), over-current protection (OCP) and over-temperature protection (OTP).

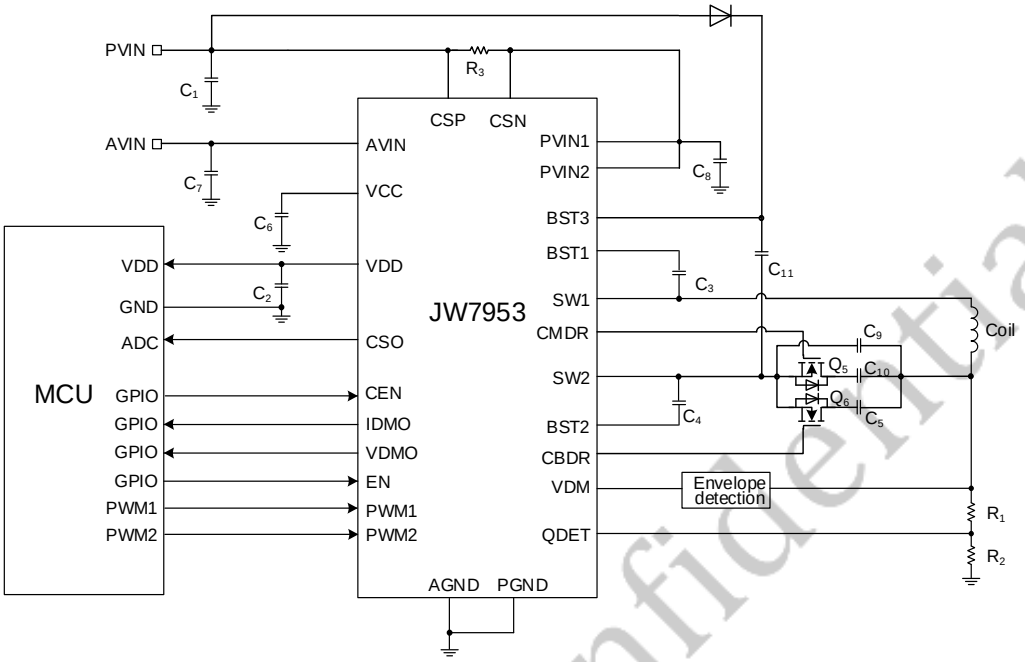
FEATURES

- Full-Bridge Input Voltage Range: 1V~20V
- LDO Input Voltage Range: 2.8V~20V
- Output power: 20W
- Integrated Four Low $R_{DS(ON)}$ FETs: 12mΩ
- Integrated 5V/50mA LDO
- Integrated 3.3V/50mA LDO
- 3.3V and 5V PWM Signal Logic Compatible
- Integrated Voltage and Current Demodulation
- Integrated Input Current Sense for FOD
- Integrated Q Factor Detection for QFOD
- Input Under-Voltage Lockout (UVLO)
- Input Over Voltage Protection (OVP)
- Over-Current Protection (OCP)
- Over-Temperature Protection (OTP)
- RoHS Compliant and Halogen Free
- Compact Package: VQFN4*4-25

APPLICATIONS

- Wireless Charger Transmitter
- Motor Drivers

TYPICAL APPLICATION

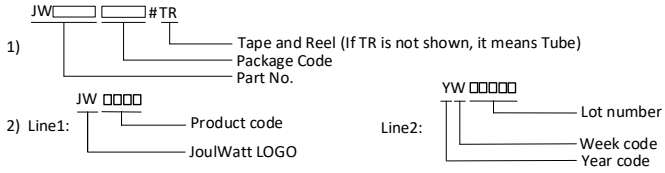


Typical Application Circuit

ORDER INFORMATION

DEVICE[1)]	PACKAGE	TOP MARKING[2)]	ENVIRONMENTAL[3)]
JW7953VQEE#TR	VQFN4*4-25	JW7953 YW□□□□□	Green

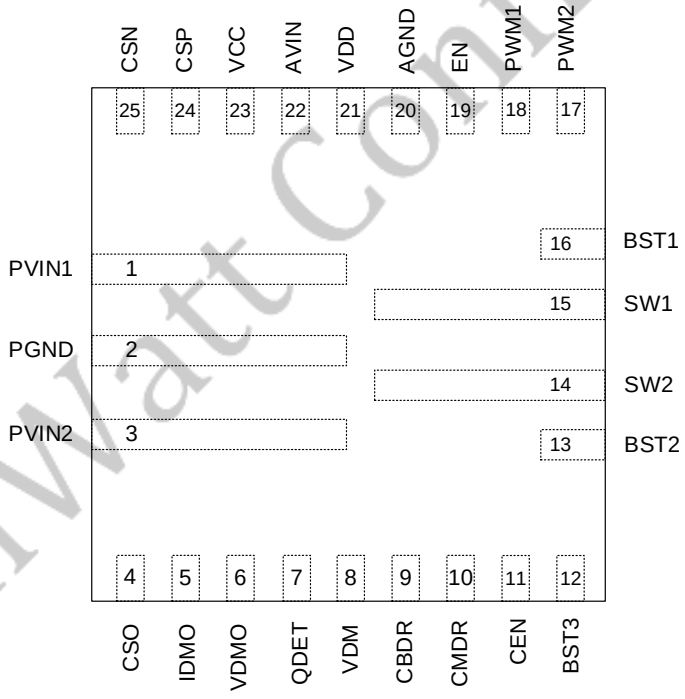
Notes:



3) All JoulWatt products are packaged with Pb-free and Halogen-free materials and compliant to RoHS standards.

PIN CONFIGURATION

TOP VIEW



VQFN4*4-25

ABSOLUTE MAXIMUM RATING (1)

PVIN1, PVIN2, AVIN, SW1, SW2, CSP, CSN .....-0.3V to 22V
BST1-SW1, BST2-SW2 .....-0.3V to 4V
BST3-SW2, CBDR-SW2, CMDR-SW2 .....-0.3V to 22V
PWM1, PWM2, VDMO, IDMO, EN, VDD, CEN..... -0.3V to 6.5V
CSO, QDET, VCC, VDM..... -0.3V to 4V
Junction Temperature Range (2) ..... -40ºC to +150ºC
Power Dissipation, P_D @ (T_A = 25ºC) (3) VQFN4*4-25 ..... TBD
Lead Temperature (Soldering, 10 sec.) 260ºC
Storage Temperature Range ..... -65ºC to +150ºC
Human-Body Model (HBM).....±2kV
Charged Device Model (CDM), per JEDEC Specification JESD22-C101.....±500V

RECOMMENDED OPERATING CONDITIONS (4)

AVIN .....2.8V to 20V
PVIN ..... 1V to 20V
Junction Temperature Range..... -40ºC to +125ºC
Ambient Temperature Range..... -40ºC to +85ºC

THERMAL PERFORMANCE (5)

	θ_{JA}	θ_{JC}
VQFN4*4-25	.....	ºC/W

Notes:

1) Exceeding these ratings may damage the device. These stress ratings do not imply function operation of the device at any other conditions beyond those indicated under RECOMMENDED OPERATIONF CONDITIONS.

2) The JW7953 includes thermal protection that is intended to protect the device in overload conditions. Continuous operation over the specified absolute maximum operating junction temperature may damage the device.

3) The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D(MAX) = (T_J(MAX)-T_A)/\theta_{JA}$.

4) The device is not guaranteed to function outside of its operating conditions.

5) Measured in the natural convection at T_A = 25ºC on the JoulWatt Evaluation Board.

ELECTRICAL CHARACTERISTICS

V_{AVIN} = V_{PVIN} = 12V, T_A = 25°C, unless otherwise specified.

Advance Information, not production data, subject to change without notice.

ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNITS
POWER SUPPLY						
LDO Operating Input Voltage	V_{AVIN}		2.8		20	V
Full-Bridge Operating Input Voltage	V_{PVIN}		1		20	V
AVIN Under-Voltage Lockout Threshold	V_{AVIN_UVLO}	V_{AVIN} rising		2.7		V
AVIN Under-Voltage Lockout Hysteresis	V_{AVIN_HYS}			100		mV
PVIN Over-Voltage Lockout Threshold	V_{PVIN_OVLO}	V_{PVIN} rising		21.5		V
PVIN Over-Voltage Lockout Hysteresis	V_{PVIN_HYS}			0.8		V
VCC UVLO Threshold	V_{VCC_UVLO}	V_{CC} rising		2.6		V
VCC UVLO Hysteresis	V_{VCC_HYS}			200		mV
Quiescent Current from AVIN Pin	I_{Q_AVIN}	VCC, VDD no Load		530	TBD	μA
Quiescent Current from PVIN1, PVIN2	I_{Q_PVIN}	EN=High, no switch		16	TBD	μA
Shutdown Current from AVIN Pin	I_{SHDN_AVIN}	EN=Low, V_{AVIN}=12V		71	TBD	μA
Shutdown Current from PVIN1, PVIN2	I_{SHDN_PVIN}	EN=Low, V_{PVIN1}=12V		3	TBD	μA
FULL-BRIDGE POWER STAGE						
High Side N-FET (HS-FET) R_{ON}	$R_{DS(ON)\_H}$	V_{BST1}-V_{SW1}=3.3V, V_{BST2}-V_{SW2}=3.3V		12	TBD	mΩ
Low Side N-FET (LS-FET) R_{ON}	$R_{DS(ON)\_L}$	V_{CC}=3.3V		12	TBD	mΩ
Switch Minimum Off Time	T_{OFF_MIN}			100		ns
Switch Minimum On Time	T_{ON_MIN}			100		ns
High Side Current Limit Threshold	I_{LIM1}	EN rising edges 0/24	TBD	10		A
	I_{LIM2}	EN rising edges 25	TBD	15		A
Hiccup Period	T_P			20		ms
GATE DRIVE OUTPUT						
Peak Source Gate Current (6)	I_{SOURCE}	$V_{CMDR/CBDR}$-V_{SW2}=12V		0.3		A
Peak Sink Gate Current (6)	I_{SINK}	$V_{CMDR/CBDR}$-V_{SW2}=0V		0.6		A

Gate Drive Pull-Up Resistance	R_{UP}			40		Ω
Gate Drive Pull-Down Resistance	R_{DOWN}			20		Ω
BST3 UVLO Threshold	V_{BST3_UVLO}	V_{BST3}-V_{SW2} rising threshold		4		V
LDO OUTPUT						
VCC Output Voltage	V_{CC}	V_{AVIN}=12V, I_{VCC}=10mA	3.21	3.3	3.39	V
VCC Current Limit	I_{VCC_LIM}			50		mA
VCC Short Current	I_{VCC_SC}			20		mA
VDD Output Voltage	V_{DD}	V_{AVIN}=12V, I_{VDD}=10mA	4.95	5	5.05	V
VDD Current Limit	I_{VDD_LIM}			50		mA
VDD Short Current	I_{VDD_SC}			20		mA
CURRENT SENSE						
CSO Current Sense Ratio	R_{CS_GAIN}	R_{CS}=10mΩ	0.495	0.5	0.505	V/A
CSO Current Sense Offset	V_{CS_OFFSET}	I_{PVIN}=0A		0.5		V
DEMODULATION						
VDM Input Hysteresis Voltage	V_{VDM_HYS1}	EN rising edges 8		8	TBD	mV
	V_{VDM_HYS2}	EN rising edges 0/9		16	TBD	mV
	V_{VDM_HYS3}	EN rising edges 10		32	TBD	mV
	V_{VDM_HYS4}	EN rising edges 11		50	TBD	mV
IDM Input Hysteresis Voltage	V_{IDM_HYS1}	EN rising edges 20		4	TBD	mV
	V_{IDM_HYS2}	EN rising edges 21		8	TBD	mV
	V_{IDM_HYS3}	EN rising edges 0/22		16	TBD	mV
	V_{IDM_HYS4}	EN rising edges 23		32	TBD	mV
Q FACTOR DETECTION						
Preset Voltage on SW1	V_{PRESET}			2.7		V
High Level Detect Voltage Threshold	V_{TH_HIGH}			200		mV
Low Level Detect Voltage Threshold	V_{TH_LOW}			100		mV
TIMING						
High Level Pulse Duration (6)	T_{HIGH}			10		μs
Low Level Pulse Duration (6)	T_{LOW}			10		μs
Turn-On Delay Time (6)	$T_{D(ON)}$	From EN high to PWM activated		3.2		ms
Turn-Off Delay Time (6)	$T_{D(OFF)}$	From EN low to chip disable		80		μs
Data Storage/Accept Time Period (6)	T_{STORE}		50			μs

LOGIC INTERFACE						
PWM1, PWM2 Logic High Threshold	V_{PWM_H}	V_{CC}=3.3V, V_{DD}=5V, Rising	2			V
PWM1, PWM2 Logic Low Threshold	V_{PWM_L}	V_{CC}=3.3V, V_{DD}=5V, Falling			0.8	V
CEN Logic High Threshold	V_{CEN_H}	V_{CC}=3.3V, V_{DD}=5V, Rising	2			V
CEN Logic Low Threshold	V_{CEN_L}	V_{CC}=3.3V, V_{DD}=5V, Falling			0.8	V
EN Logic High Threshold	V_{EN_H}	V_{CC}=3.3V, V_{DD}=5V, Rising	2			V
EN Logic Low Threshold	V_{EN_L}	V_{CC}=3.3V, V_{DD}=5V, Falling			0.8	V
VDMO, IDMO Output Logic High	$V_{DMO\_H\_VDD}$	EN rising edges 0/19	0.9*VDD			V
VDMO, IDMO Output Logic Low	$V_{DMO\_L\_VDD}$	EN rising edges 0/19			0.1*VDD	V
VDMO, IDMO Output Logic High	$V_{DMO\_H\_VCC}$	EN rising edges 18	0.9*VCC			V
VDMO, IDMO Output Logic Low	$V_{DMO\_L\_VCC}$	EN rising edges 18			0.1*VCC	V
PROTECTION						
Thermal Shutdown Temperature (6)	T_{SD}			150		ºC
Thermal Shutdown Hysteresis (6)	T_{HYS}			15		ºC

Note:

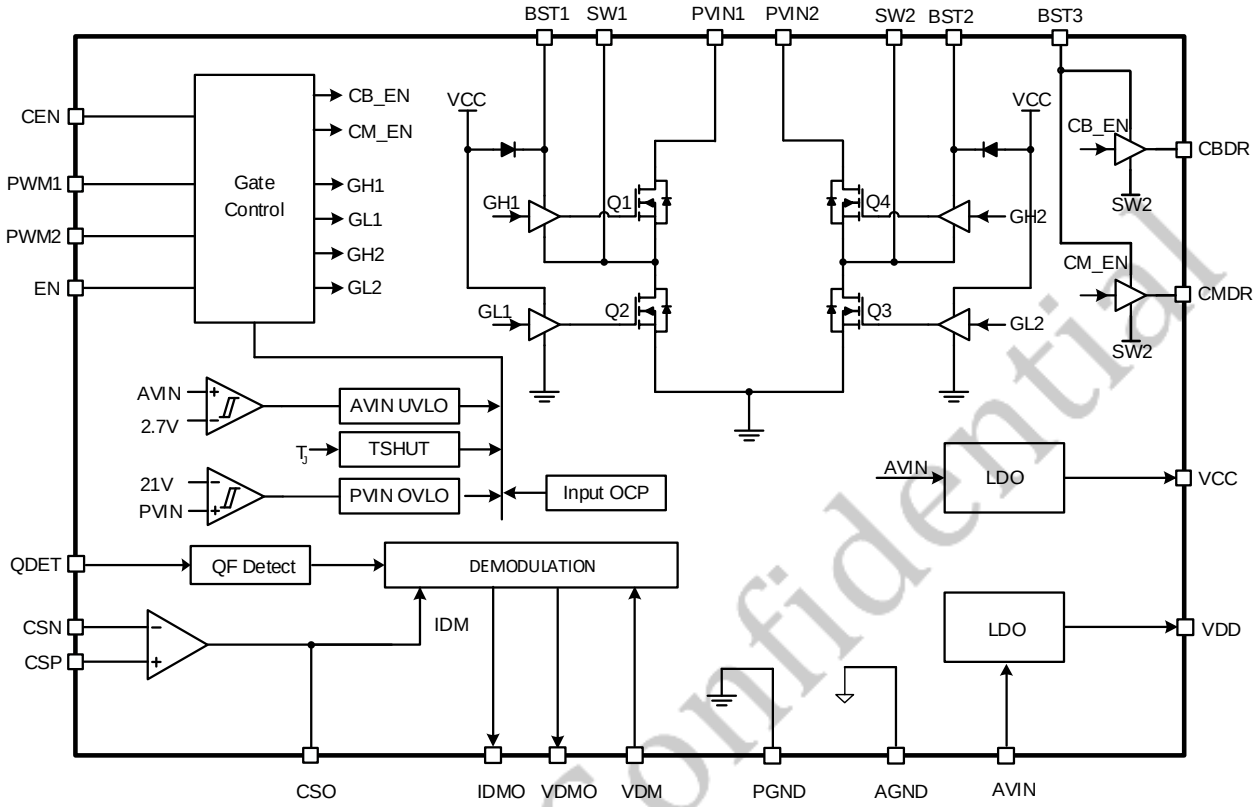
6) Guaranteed by design.

PIN DESCRIPTION

PIN NO.	NAME	DESCRIPTION
1	PVIN1	Input voltage for half-bridge MOSFET. Bypass with a 22μF ceramic capacitor to PGND.
2	PGND	Power ground.
3	PVIN2	Input voltage for half-bridge MOSFET. Bypass with a 22 μF ceramic capacitor to PGND.
4	CSO	Input current sense output pin.
5	IDMO	Output of the demodulated 2kHz communication signal based on current demodulation scheme.
6	VDMO	Output of the demodulated 2kHz communication signal based on voltage demodulation scheme. When enabling Q-value detection, VDMO pin serves as the output pin for Q-value detection.
7	QDET	Quality factor detection input.
8	VDM	High-pass filter input. Voltage demodulation pin for data packets based on coil voltage variation.
9	CBDR	Driver for Q6 which switching resonant capacitors.
10	CMDR	Driver for Q5 which switching resonant capacitors.
11	CEN	Tri-state control pin for CBDR and CMDR. If the CEN pin is high, both CBDR and CMDR output high. If the CEN pin is low, both CBDR and CMDR output low. If the CEN pin is high-Z, CMDR outputs high and CBDR outputs low.
12	BST3	Bootstrapped supplies to the high side floating driver of Q5 and Q6. An 0.1μF ceramic capacitor is suggested to be connected between this pin and the SW2 pin.
13	BST2	Bootstrapped supplies to the high side floating driver of Q4. An 0.1μF ceramic capacitor is suggested to be connected between this pin and the SW2 pin.
14	SW2	Power switching node 2.
15	SW1	Power switching node 1.
16	BST1	Bootstrapped supplies to the high side floating driver of Q1. An 0.1μF ceramic capacitor is suggested to be connected between this pin and the SW1 pin.
17	PWM2	PWM input for the control of the arm at SW2 side. When PWM2 is high, the top switch Q4 is turned on and the bottom switch Q3 is turned off. When PWM2 is low, the top switch Q4 is turned off and the bottom switch Q3 is turned on.
18	PWM1	PWM input for the control of the arm at SW1 side. When PWM1 is high, the top switch Q1 is turned on and the bottom switch Q2 is turned off. When PWM1 is low, the top switch Q1 is turned off and the bottom switch Q2 is turned on.
19	EN	Chip enable pin. Active high to enable the chip. When EN is low, the chip is disabled, and both SW1 and SW2 are pulled down to PGND for about 365μs, and then change to high-Z.

20	AGND	Analog ground.
21	VDD	5V LDO for internal circuits and external MCU. Connect a 2.2μF ceramic capacitor from VDD to AGND.
22	AVIN	Input voltage for internal 5V LDO and 3.3V LDO. Bypass with a 10μF ceramic capacitor to AGND.
23	VCC	3.3V LDO for internal gate drivers, control circuits and external MCU. Connect a 2.2μF ceramic capacitor from VCC to AGND.
24	CSP	Positive terminal of input current sense.
25	CSN	Negative terminal of input current sense.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

JW7953 is a high-efficiency full-bridge power stage (integrated MOS plus driver) with voltage/current demodulation and LDO for wireless charger transmitter. With a transmitter controller, it can provide flexible wireless transmitter solutions, compliant with Qi v2.0 Baseline Power Profile (BPP), Extended Power Profile (EPP) and Magnetic Power Profile (MPP).

Integrated Full-Bridge Stage

The JW7953 integrates a full-bridge power stage with low $R_{DS(ON)}$ (typical 12mΩ) N-channel MOSFETs and can work with wide input voltage range from 1.0V to 20V. All circuits needed to drive the full-bridge stage are integrated, such as gate driver and bootstrap circuits. With the PWM control signals from the controller, it can be widely used in wireless transmitter applications.

PWM Control

The JW7953 has two PWM input pins, PWM1 and PWM2. Each input signal can control one arm of the integrated full-bridge independently. The PWM1 input controls the arm of Q1 and Q2, and the PWM2 input controls the arm of Q3 and Q4.

When the input PWM signal is high, the top switch of the corresponding arm is turned on, and the bottom switch of this arm is turned off. When the input PWM signal is low, the bottom switch of the corresponding arm is turned on, and the top switch of this arm is turned off. For example, when PWM1 is high, the Q1 is turned on and the Q2 is turned off. When PWM1 is low, the Q1 is turned off and the Q2 is turned on.

For a typical WPC transmitter, the PWM1 and the PWM2 are complementary and the duty cycle is fixed in 50% with the frequency range from 100kHz to 1MHz.

Current Sense

The JW7953 provides input current sense function. The total input current is measured by the current sensing resistor and reported on the CSO pin.

The integrated current sense amplifier has voltage gain of 50V/V. For proper scaling of the current signal, the recommended current sense resistor is 10mΩ/20mΩ. The current sense amplifier output has a fixed 0.5V (typical) offset when the sensed current is zero. For accurate measurement of the input current, MCU needs to calibrate this offset.

The output voltage of CSO pin can be calculated by the formula below.

$$V_{CSO}(V) = 0.5V + R_{CS}(\Omega) \times 50 \times I_{PVIN}(A)$$

LDO

The JW7953 has two integrated low-dropout (LDO) voltage regulators. VCC pin is 3.3V LDO output and VDD pin is 5V LDO output. The internal power drivers and control circuits are powered from the VCC. The load capability of VDD/VCC regulator is about 50mA, so it can be used to power up MCU and LED directly. Customers can choose to use 3.3V or 5V power supply according to the application.

The VCC and VDD regulator is not controlled by the EN signal.

Voltage Demodulation

In order to increase the communication reliability in any load condition, the JW7953 has integrated two demodulation schemes, one based on input average current information and the other based

on coil voltage information. The voltage mode envelope detector is implemented using a discrete solution as depicted on Figure 1. This simple implementation achieves the envelope detector function low-pass filter as well as the DC filter function.

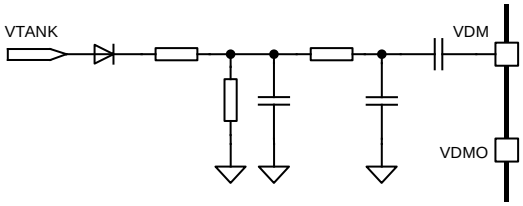


Figure 1: Voltage Demodulation Peripheral Circuit

Current Demodulation

The current-mode detector takes the modulation information from the average input current. The input signal of current demodulation is CSO pin. The 2kHz data signal carried by the input current is demodulated through the internal current demodulation circuit.

The MCU can detect the demodulation results on the VDMO and the IDMO pins and then implement the packet decode. The MCU can select either voltage-mode or current-mode signals depending upon which produces the best demodulated signal.

Q Factor Detection

The JW7953 integrates an accurate Q factor detection circuit to implement foreign objects detection before the selection phase. When a metal foreign object is placed on the charging surface of T_X, the quality factor of the resonant circuit composed of coil, resonant capacitance and parasitic resistance will decrease. Set a reasonable quality factor threshold to judge whether there is metal foreign matter on the surface of the coil.

After Q detection is enabled, MCU can calculate the Q of T_X according to the number of pulses on the VDMO pin, and then judge whether there is metal foreign objects on the charging surface of T_X before the selection stage.

The calculation formula of Q value is as follows.

$$Q = \frac{N \bullet \pi}{ln(\frac{V_{HIGH}}{V_{LOW}})}$$

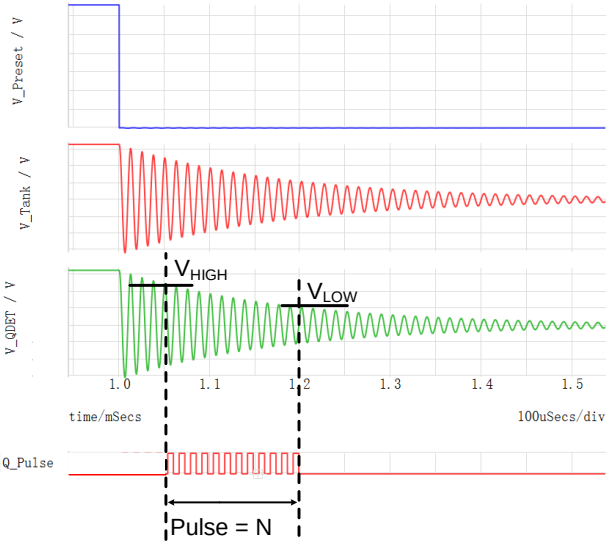


Figure 2: Q Factor Detection Diagram

Drivers for Switchable Resonant Capacitor

If MPP is supported, the system will operate at a fixed power transmission frequency of 360 kHz. This operating frequency exceeds the existing BPP frequency range, so different resonant capacitors on PTx and PRx are required to achieve efficient power transmission. Therefore, both PTx and PRx have switchable resonant capacitor banks to support MPP and BPP.

The JW7953 integrates two drivers for switchable resonant capacitor, which can drive external NMOS directly. If the CEN pin is high, CMDR and

CBDR output high. If the CEN pin is low, CMDR and CBDR output low. If the CEN pin is high-Z, the CMDR outputs high and CBDR outputs low as shown in Table 1. CEN needs to be programmed when there is no energy stored in the resonant circuit to avoid damaging the IC and the external MOSFETs.

Table 1: CEN Control Table

CEN	CMDR	CBDR
High	High	High
Low	Low	Low
High Z	High	Low

Digital Interface (EN pin)

The digital interface is mainly used for Q factor detection function and some configuration. If the digital interface is not required, this pin can also be used as a standard enable pin (EN pin). The H-bridge starts operating about $T_{D(ON)}$ (Typ. 3.2ms) after the first EN rising edge. Once the device is enabled, Q factor detection is not implemented. The digital interface counts the rising edges applied to the EN pin and enables the new function according to Table 2.

Table 2: Programming Table

Rising Edges	Function
8	V_{VDM_HYS} = 8mV
0/9	V_{VDM_HYS} = 16mV
10	V_{VDM_HYS} = 32mV
11	V_{VDM_HYS} = 50mV
12	Enable Q factor detection
0/13	Disable Q factor detection
14	Driver speed slowest
15	Driver speed slow
16	Driver speed medium
0/17	Driver speed fast
18	Set the VDMO/IDMO logic voltage to VCC
0/19	Set the VDMO/IDMO logic voltage to VDD
20	V_{IDM_HYS} = 4mV
21	V_{IDM_HYS} = 8mV
22	V_{IDM_HYS} = 16mV
23	V_{IDM_HYS} = 32mV
0/24	I_{LIM} = 10A
25	I_{LIM} = 15A

In order to realize the digital interface function of the EN pin, the high level and the low level between two adjacent rising edges need to keep for T_{HIGH} (Typ. 10μs) and T_{LOW} (Typ. 10μs).

After the EN pulses, the high level shall be maintained at least T_{STORE} (Min. 50μs) to enable the corresponding function. At the same time, the rising edge counter is set to 0, and EN can continue to pulse to enable the next function. That is, between the enabling of the two functions, the EN pin shall keep high level for least T_{STORE} (Min. 50μs).

After the EN pin remains low level for $T_{D(OFF)}$ (Typ. 80μs), the chip shuts down and all functions return to the default state. As shown in the Figure 3.

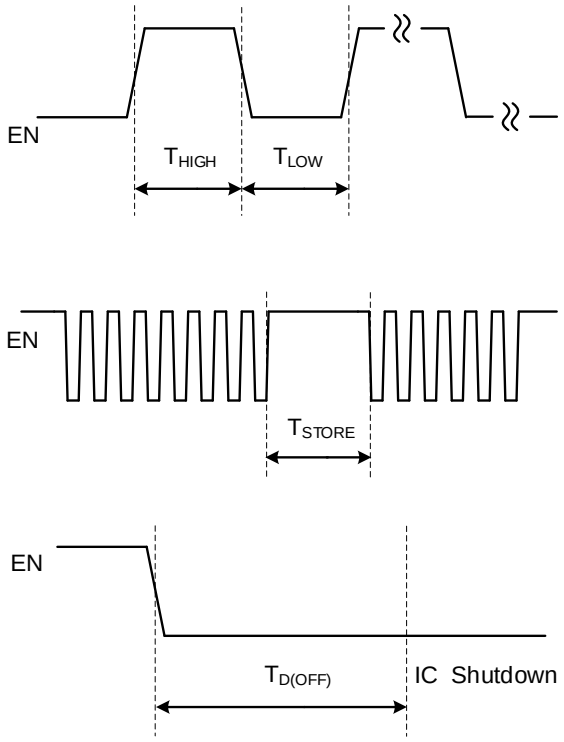


Figure 3: EN Digital Interface Waveform Diagram

Protection

The JW7953 guarantees robustness with over-current protection, over-temperature protection, under-voltage lockout and input over-voltage protection.

Over-Current Protection

The JW7953 measures the inductance peak current by two top switches. And the over-current protection threshold is constant 10A (**option 15A**).

When the inductance peak current exceeds the over-current threshold, the device turns off the top switches and turns on the bottom switches regardless of the status of PWM1 and PWM2 to protect the chip from damaging. When the over-current event happens 4 times, IC will enter hiccup mode.

Under-Voltage Lockout

When the V_{AVIN} falls below the V_{AVIN_UVLO} falling threshold, the device stops switching. When the V_{AVIN} rises above the V_{AVIN_UVLO} rising threshold, the device resumes working, if EN is still high.

Input Over-Voltage Protection

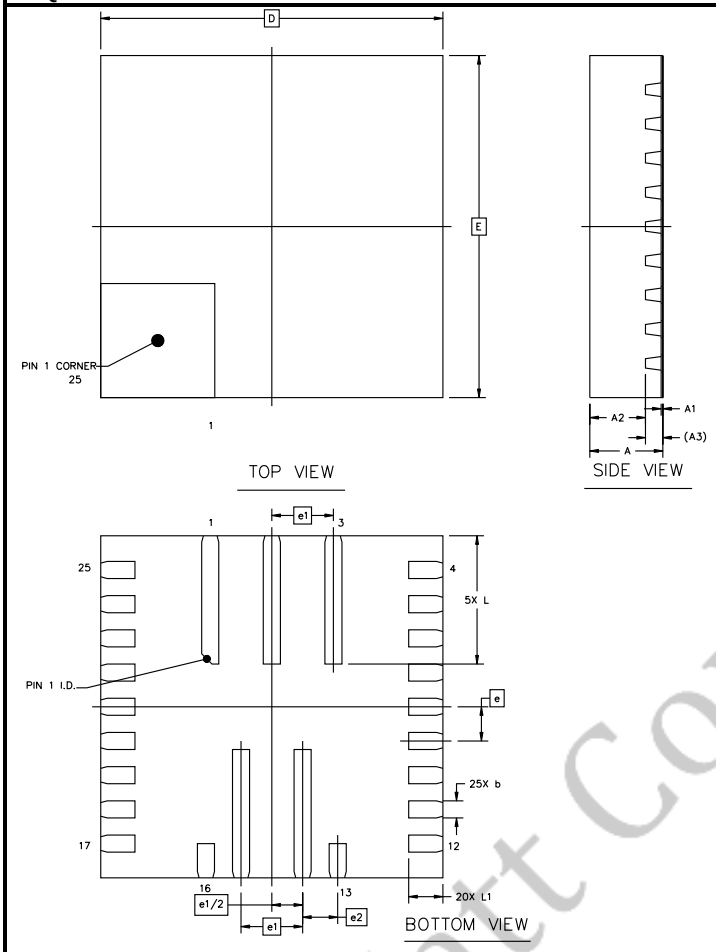
When the V_{PVIN} rises above the V_{PVIN_OVLO} rising threshold, the device stops switching. When the V_{PVIN} falls below the V_{PVIN_OVLO} falling threshold, the device resumes working, if EN is still high and V_{AVIN} is still above the V_{AVIN_UVLO} falling threshold.

Over-Temperature Protection

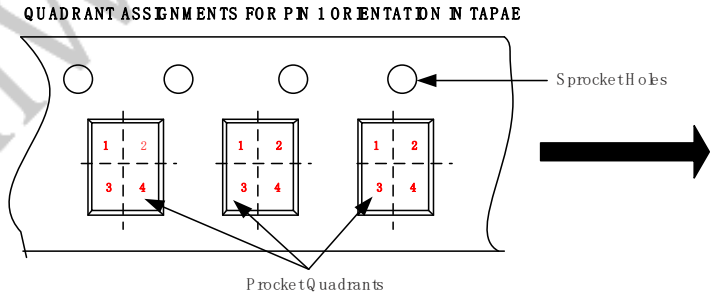
When the junction temperature of the JW7953 rises above 150°C, the device enters thermal shut down mode. When the temperature of the JW7953 drops below 135°C, the JW7953 can be resumed.

PACKAGE OUTLINE

VQFN4*4-25 UNIT: mm



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A2	-	0.65	-
A3	0.203 REF		
b	0.15	0.20	0.25
D	3.90	4.00	4.10
E	3.90	4.00	4.10
e	0.4 BSC		
e1	0.72 BSC		
e2	0.41 BSC		
L	1.40	1.50	1.60
L1	0.30	0.40	0.50



Package Type	Pin1 Quadrant
VQFN4*4-25	1

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REVISION HISTORY

REV	DATE	DESCRIPTION
Rev 0.1	01/20/2025	1. Initial revision