JW7952

20W Full-Bridge with Demodulation and LDO for the Wireless Charger Transmitter

Preliminary Specifications Subject to Change without Notice

DESCRIPTION

The JW7952 is a high efficiency full-bridge power stage with voltage/current demodulation designed for wireless charger transmitter. With a transmitter controller, it can provide flexible wireless charger solutions complaint with Qi v1.2.4 and Qi v1.3 Baseline Power Profile (BPP) and Extended Power Profile (EPP).

The JW7952 integrates a 4-MOSFETs full bridge with low $R_{DS(ON)}$, gate drivers, 5V LDO, 3.3V LDO, input current sensor , voltage/current communication demodulation, Q factor detection and protection circuit.

The JW7952 provides input current sense function. The chip measures the input current with the current sampling resistor and reports it on the CSO pin, so that the transferred power can be detected by the controller. The controller realizes foreign object detection (FOD) by continuously monitoring transferred power and received power. For EPP equipment, Q factor detection is required to realize foreign object protection by comparing with the set Q threshold.

The JW7952 guarantees robustness with under voltage lockout (UVLO), input over voltage protection(OVLO), over current protection (OCP) and thermal shutdown(OTP).

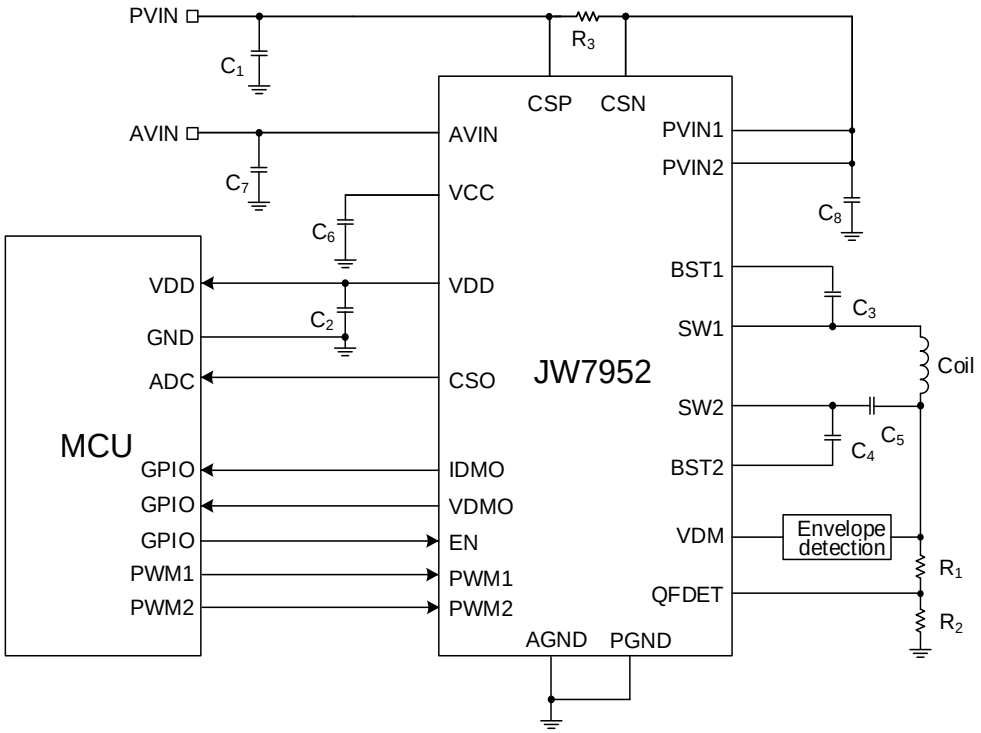
FEATURES

- Full Bridge Input Voltage Range: 2V~14V
- LDO Input Voltage Range: 2.8V~20V
- Output power: 20W
- Integrated Four Low $R_{DS(ON)}$ FETs : 12mΩ
- Integrated 5V/50mA LDO
- Integrated 3.3V/50mA LDO
- 3.3V and 5V PWM Signal Logic Compatible
- Integrated voltage and current demodulation
- Integrated input current sense for FOD
- Integrated Q factor detection for QFOD
- Under Voltage Lockout (UVLO)
- Input Over Voltage Protection(OVLO)
- Over Current Protection(OCP)
- Thermal Shutdown(OTP)
- RoHS Compliant and Halogen Free
- Compact Package: VQFN3x3.5-21

APPLICATIONS

- Wireless Charger Transmitter
- Motor Drivers

TYPICAL APPLICATION



Typical application circuit

ORDER INFORMATION

DEVICE[1)]	PACKAGE	TOP MARKING[2)]	ENVIRONMENTAL[3)]
JW7952VQBFX#TR	VQFN3x3.5-21	JW7952 YW□□□□□	Green

Notes:

1) JW□□□□#TR
- Tape and Reel (If TR is not shown, it means Tube)
- Package Code
- Part No.

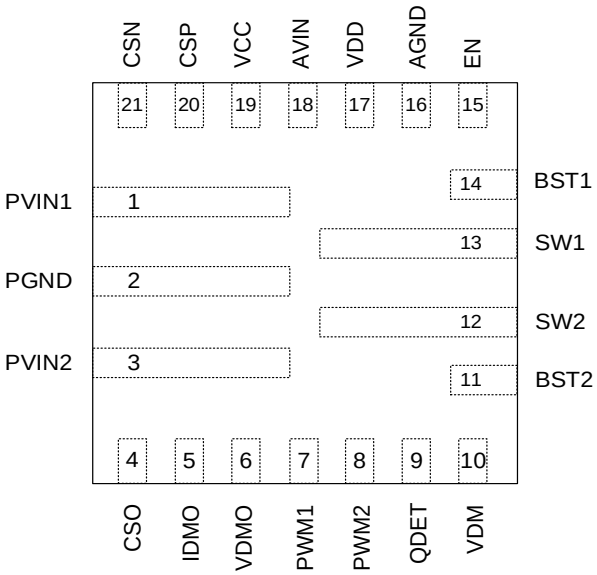
2) Line1: JW □□□□
- Product code
- JoulWatt LOGO

Line2: YW □□□□□
- Lot number
- Week code
- Year code

3) All JoulWatt products are packaged with Pb-free and Halogen-free materials and compliant to RoHS standards.

PIN CONFIGURATION

TOP VIEW



VQFN3×3.5-21

ABSOLUTE MAXIMUM RATING[1)]

PVIN1, PVIN2, SW1,SW2, CSP, CSN .....-0.3V to 16.5V
AVIN ..... -0.3V to 22V
BST1-SW1, BST2-SW2 .....-0.3V to 4V
PWM1, PWM2, VDMO, IDMO, EN, VDD ..... -0.3V to 6.5V
CSO, QDET, VCC,VDM..... -0.3V to 4V

Junction Temperature Range[2] ..... -40ºC to +150ºC
Power Dissipation, P_D @ (T_A = 25ºC) [3] VQFN3×3.5-21 ..... TBD
Lead Temperature (Soldering, 10 sec.) 260ºC
Storage Temperature Range ..... -65ºC to +150ºC
Human-body model(HBM).....±2kV
Charged device model(CDM),per JEDEC specification JESD22-C101.....±500V

RECOMMENDED OPERATING CONDITIONS[4]

AVIN .....2.8V to 20V
PVIN ..... 2V to 14V
Junction Temperature Range ..... -40ºC to +125ºC
Ambient Temperature Range ..... -40ºC to +85ºC

THERMAL PERFORMANCE[5]

	θ_{JA}	θ_{JC}
VQFN3×3.5-21	.....	ºC/W

Note:

1) Exceeding these ratings may damage the device. These stress ratings do not imply function operation of the device at any other conditions beyond those indicated under RECOMMENDED OPERATIONF CONDITIONS

2) The JW7952 includes thermal protection that is intended to protect the device in overload conditions. Continuous operation over the specified absolute maximum operating junction temperature may damage the device.

3) The maximum allowable continuous power dissipation at any ambient temperature is calculated by PD (MAX) = (T_J(MAX)-T_A)/θ_{JA}.

4) The device is not guaranteed to function outside of its operating conditions.

5) Measured in the natural convection at T_A = 25℃ on the JoulWatt Evaluation Board.

ELECTRICAL CHARACTERISTICS

V_{AVIN}=12V, T_A=25°C, unless otherwise specified.

Advance Information, not production data, subject to change without notice.

Item	Symbol	Condition	Min.	Typ.	Max.	Units
POWER SUPPLY						
LDO Operating Input Voltage	V_{AVIN}		2.8		20	V
Full-Bridge Operating Input Voltage	V_{PVIN}		2		14	V
AVIN Under Voltage Lockout Threshold	V_{AVIN_UVLO}	V_{AVIN} rising		2.73		V
AVIN Under Voltage Lockout Hysteresis	V_{AVIN_HYS}			203		mV
PVIN Over Voltage Lockout Threshold	V_{PVIN_OVLO}	V_{PVIN} rising		16		V
PVIN Over Voltage Lockout Hysteresis	V_{PVIN_HYS}			0.824		V
VCC UVLO Threshold	V_{VCC_UVLO}	V_{CC} rising		2.62		V
VCC UVLO Hysteresis	V_{VCC_HYS}			209		mV
Quiescent Current from AVIN Pin	I_{Q_AVIN}	VCC,VDD no Load		534		uA
Quiescent Current from PVIN1, PVIN2	I_{Q_PVIN}	EN=high,no switch		15.7		uA
Shutdown Current from AVIN Pin	I_{SHDN_AVIN}	EN=low, V_{AVIN}=12V		90.1		uA
Shutdown Current from PVIN1, PVIN2	I_{SHDN_PVIN}	EN=low, V_{PVIN1}=12V		0.15	3	uA
FULL BRIDGE POWER STAGE						
High Side N-FET(LS-FET) R_{ON}	$R_{DS(ON)\_H}$	V_{BST1}-V_{SW1}=3.3V, V_{BST2}-V_{SW2}=3.3V		12		mΩ
Low Side N-FET(HS-FET) R_{ON}	$R_{DS(ON)\_L}$	V_{CC}=3.3V		12		mΩ
Switch Minimum off Time	T_{off_min}			120		ns
Switch Minimum on Time	T_{on_min}			120		ns
How Side Current Limit Threshold	I_{LIM}			12.95		A
Hiccup Period	T_p			20		ms
LDO OUTPUT						
VCC Output Voltage	V_{CC}	V_{AVIN}=12V, I_{VCC}=10mA	3.24	3.3	3.37	V
VCC Current Limit	I_{VCC_LIM}			62		mA
VCC Short Current	I_{VCC_SC}			21		mA
VDD Output Voltage	V_{DD}	V_{AVIN}=12V, I_{VDD}=10mA	4.92	5	5.13	V
VDD Current Limit	I_{VDD_LIM}			62		mA
VDD Short Current	I_{VDD_SC}			21		mA
CURRENT SENSE						
CSO Current Sense Ratio	R_{CS_Gain}	R_{CS}=10mΩ	0.497	0.5	0.502	V/A
CSO Current Sense Offset	V_{CS_Offset}	I_{PVIN}=0A		0.51		V

DEMODULATION						
VDM Input Hysteresis Voltage	V_{VDM_HYS}			22		mV
IDM Input Hysteresis Voltage	V_{IDM_HYS}			14		mV
Q FACTOR DETECTION						
Preset Voltage Threshold on SW1	V_{TH_PRESET}			2.5		V
High Level Detect Voltage Threshold	V_{TH_HIGH}			200		mV
Low Level Detect Voltage Threshold	V_{TH_LOW}			100		mV
TIMING						
High-level Pulse Duration(6)	T_{HIGH}			10		us
Low-level Pulse Duration(6)	T_{LOW}			10		us
Turn-off Delay Time(6)	$T_{D(OFF)}$			80		us
Data Storage/Accept Time Period(6)	T_{STORE}		50			us
LOGIC INTERFACE						
PWM1, PWM2 Logic High Threshold	V_{PWM_H}	V_{CC}=3.3V,V_{DD}=5V, Input Rising	2			V
PWM1, PWM2 Logic Low Threshold	V_{PWM_L}	V_{CC}=3.3V,V_{DD}=5V, Input Falling			0.8	V
EN Logic High Threshold	V_{EN_H}	V_{CC}=3.3V,V_{DD}=5V, EN Rising	2			V
EN Logic Low Threshold	V_{EN_L}	V_{CC}=3.3V,V_{DD}=5V, EN Falling			0.8	V
VDMO,IDMO Output Logic High	$V_{DMO\_H\_VDD}$	EN Rising Edges 19/0	0.9*VDD			V
VDMO,IDMO Output Logic Low	$V_{DMO\_L\_VDD}$	EN Rising Edges 19/0			0.1*VDD	V
VDMO,IDMO Output Logic High	$V_{DMO\_H\_VCC}$	EN Rising Edges 18	0.9*VCC			V
VDMO,IDMO Output Logic Low	$V_{DMO\_L\_VCC}$	EN Rising Edges 18			0.1*VCC	V
PROTECTION						
Thermal Shutdown Temperature(6)	T_{SD}			155		ºC
Thermal Shutdown Hysteresis(6)	T_{HYS}			15		ºC

Note:

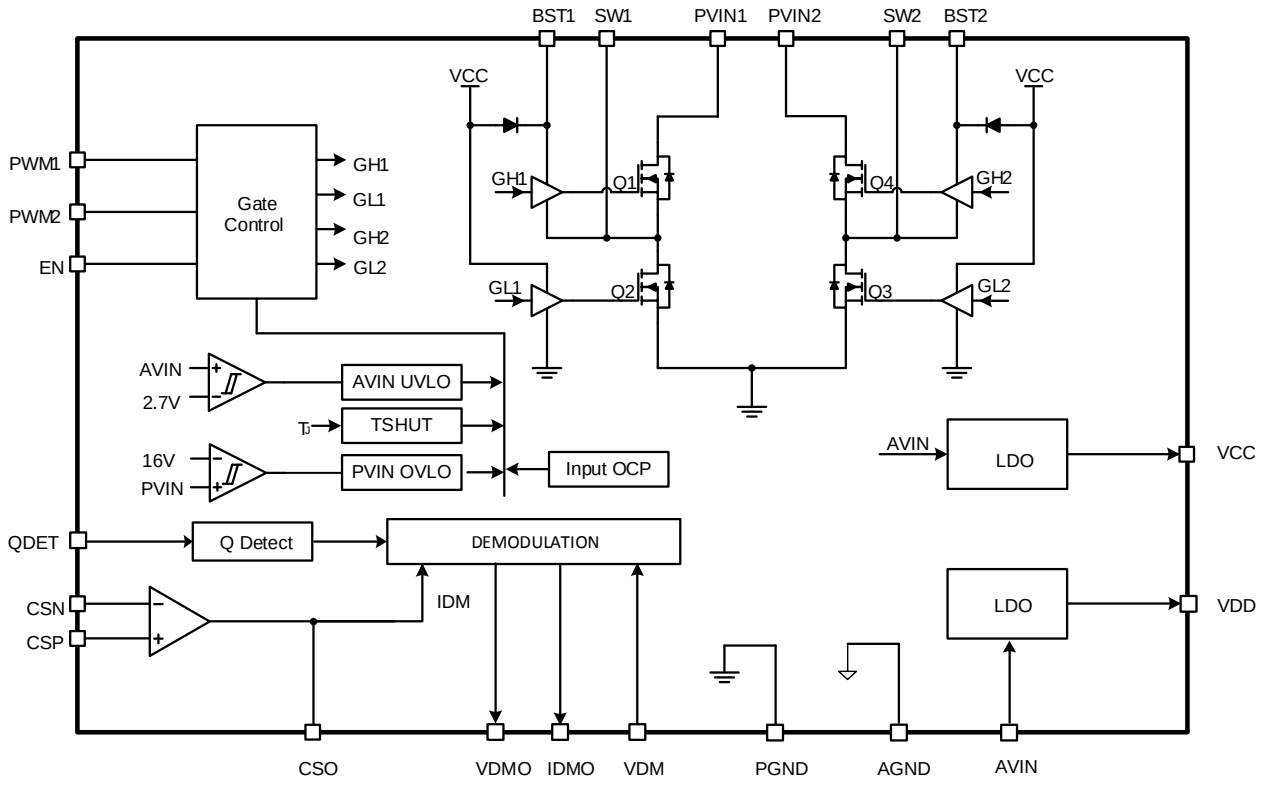
6) Guaranteed by design.

PIN DESCRIPTION

Pin No.	Name	Description
1	PVIN1	Input voltage for half-bridge MOSFET. Bypass with a 22 µF ceramic capacitor to PGND.
2	PGND	Power ground.
3	PVIN2	Input voltage for half-bridge MOSFET. Bypass with a 22 µF ceramic capacitor to PGND.
4	CSO	Input current sense output pin.
5	IDMO	Output of the demodulated 2-kHz communication signal based on current demodulation scheme.
6	VDMO	Output of the demodulated 2-kHz communication signal based on voltage demodulation scheme.
7	PWM1	PWM input for the control of the arm at SW1 side. When PWM1 is high, the top switch Q1 is turned on and the bottom switch Q2 is turned off. When PWM1 is low, the top switch Q1 is turned off and the bottom switch Q2 is turned on.
8	PWM2	PWM input for the control of the arm at SW2 side. When PWM2 is high, the top switch Q4 is turned on and the bottom switch Q3 is turned off. When PWM2 is low, the top switch Q4 is turned off and the bottom switch Q3 is turned on.
9	QDET	Quality factor detection input.
10	VDM	High-pass filter input. Voltage demodulation pin for data packets based on coil voltage variation.
11	BST2	Bootstrapped supplies to the high side floating driver of Q4. An 0.1µF ceramic capacitor is suggested to be connected between this pin and SW2 pin.
12	SW2	Power switching node 2.
13	SW1	Power switching node 1.
14	BST1	Bootstrapped supplies to the high side floating driver of Q1. An 0.1µF ceramic capacitor is suggested to be connected between this pin and SW1 pin.
15	EN	Chip enable pin. Active High to enable the chip. When EN is low, the chip is disabled, and both SW1 and SW2 are pulled down to PGND for about 200us, and then change to high-Z.
16	AGND	Analog Ground.
17	VDD	5.0V LDO for internal circuits and external MCU. Connect a 2.2 µF ceramic capacitor from VDD to AGND.
18	AVIN	Input voltage for internal 5.0V LDO and 3.3V LDO, Bypass with a 10 µF ceramic capacitor to AGND.

19	VCC	3.3V LDO for internal gate drivers ,control circuits and external MCU. Connect a 2.2 µF ceramic capacitor from VCC to AGND.
20	CSP	Positive terminal of input current sense.
21	CSN	Negative terminal of input current sense.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

JW7952 is a high-efficiency full-bridge power stage (integrated MOS plus driver) with voltage/current demodulation and LDO for wireless charger transmitter. With a transmitter controller, it can provide flexible wireless transmitter solutions, compliant with Qi v1.2.4 and Qi v1.3 Baseline Power Profile and Extended Power Profile.

Integrated Full-Bridge Stage

The JW7952 integrates a full-bridge power stage with low R_{DSON} (typical 12mΩ) N-channel MOSFETs and can work with wide input voltage ranging from 1.0V to 14V. All circuits needed to drive the full-bridge stage are integrated, such as gate driver and bootstrap circuits. With the PWM control signals from the controller, it can be widely used in wireless transmitter applications.

PWM Control

The JW7952 has two PWM input pins, PWM1 and PWM2. Each input signal can control one arm of the integrated full-bridge independently. The PWM1 input controls the arm of Q1 and Q2, and the PWM2 input controls the arm of Q3 and Q4.

When the input PWM signal is high, the top switch of the corresponding arm is turned on, and the bottom switch of this arm is turned off. When the input PWM signal is low, the bottom switch of the corresponding arm is turned on, and the bottom switch is turned off. For example, when PWM1 is high, the Q1 is turned on and Q2 is turned off. When PWM1 is low the Q1 is turned off and Q2 is turned on.

For a typical WPC transmitter, the PWM1 and PWM2 are complementary and the duty cycle is fixed in 50% with the frequency range from 100kHz to 205kHz. When the frequency reaches 205kHz, the output power can be limited furtherly by reducing the duty cycle of PWM1 and PWM2.

Current Sense

The JW7952 provides input current sense function. The total input current is measured by the current sensing resistor and reported on CSO pin.

The integrated current sense amplifier has voltage gain of 50 V/V. For proper scaling of the current signal, the recommended current sense resistor is 10mΩ/20mΩ. The current sense amplifier output has a fixed 0.5V (typical) offset when the sensed current is zero. For accurate measurement of the input current, MCU need to calibrate this offset.

The output voltage of CSO pin can be calculated by the formula below.

$$V_{CSO}(V) = 0.5V + R_{CS}(\Omega) \times 50 \times I_{PVIN}(A)$$

LDO

The JW7952 has two integrated low-dropout (LDO) voltage regulators. VCC pin is 3.3V LDO output and VDD pin is 5V LDO output. The internal power drivers and control circuits are powered from the VCC. The load capability of VDD/VCC regulator is about 50mA, so it can be used to power up MCU and LED directly. Customers can choose to use 3.3V or 5V power supply according to the application.

The VCC and VDD regulator is not controlled by the EN signal.

Voltage Demodulation

In order to increase the communication reliability in any load condition, the JW7952 has integrated

two demodulation schemes, one based on input average current information and the other based on coil voltage information. The voltage mode envelope detector is implemented using a discrete solution as depicted on Figure1. This simple implementation achieves the envelope detector function low-pass filter as well as the DC filter function.

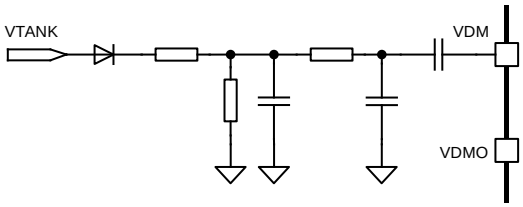


Figure 1. Voltage Demodulation peripheral circuit

Current Demodulation

The current-mode detector takes the modulation information from the average input current. The input signal of current demodulation is CSO pin. The 2KHz data signal carried by the input current is demodulated through the internal current demodulation circuit.

The MCU can detect the demodulation results on VDMO and IDMO pins and then implement the packet decode. The MCU can select either voltage-mode or current-mode signals depending upon which produces the best demodulated signal.

Q Factor Detection

The JW7952 integrates an accurate Q factor detection circuit to implement foreign objects detection before the selection phase. When a metal foreign object is placed on the charging surface of T_X, the quality factor of the resonant circuit composed of coil, resonant capacitance and parasitic resistance will decrease. Set a reasonable quality factor threshold to judge whether there is metal foreign matter on the surface of the coil.

After Q detection is enabled, MCU can calculate the Q of TX according to the number of pulses on VDMO pin, and then judge whether there is metal foreign objects on the charging surface of T_X before the selection stage.

The calculation formula of Q value is as follows.

$$Q = \frac{N \bullet \pi}{ln(\frac{V_{HIGH}}{V_{LOW}})}$$

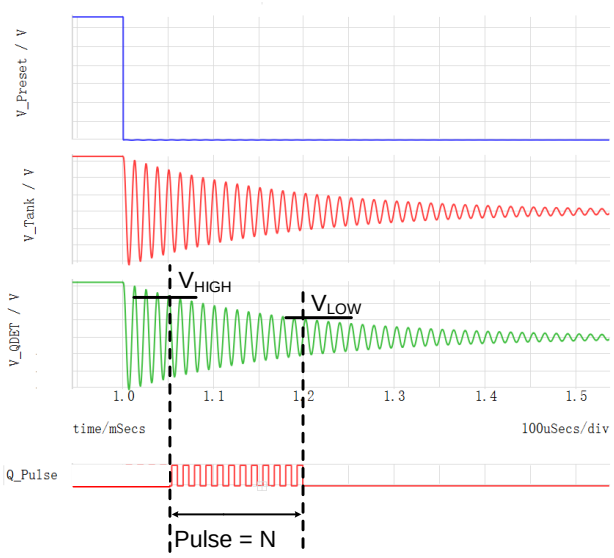


Figure 2. Q Factor detection diagram

Digital Interface (EN pin)

The digital interface is used to Q factor detection function. If digital interface is not required, the EN pin can also be used as a standard enable pin. Once the device is enabled, Q factor detection is not implemented. The interface counts the rising edges applied to the EN pin and enable the new function according to Table 1.

Table 1 Programming Table

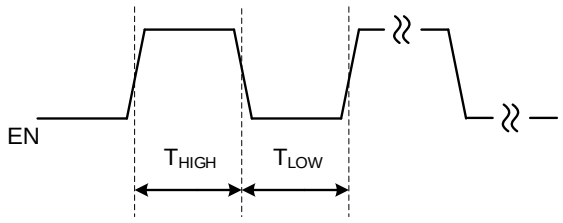
Rising Edges	Function
13	Enable Q factor detection

0/14	Disable Q factor detection
15	Driver speed slowest
16	Driver speed slow
0/17	Driver speed fast
18	Set the VDMO/IDMO logic voltage to VCC
0/19	Set the VDMO/IDMO logic voltage to VDD

In order to realize the digital interface function of EN pin, the high level and the low level between two adjacent rising edges need to keep for T_{HIGH}(Typ. 10us) and T_{LOW}(Typ. 10us).

After the EN pulses, the high level shall be maintained at least T_{STORE} (Min. 50us) to enable the corresponding function. At the same time, the rising edge counter is set to 0, and EN can continue to pulse to enable the next function. That is, between the enabling of the two functions, the EN shall keep high level for least T_{STORE}(Min. 50us).

After the EN remains low level for $T_{D(OFF)}$ (Typ 80us), the chip will shut down and all functions will return to the default state. As shown in the figure 3.



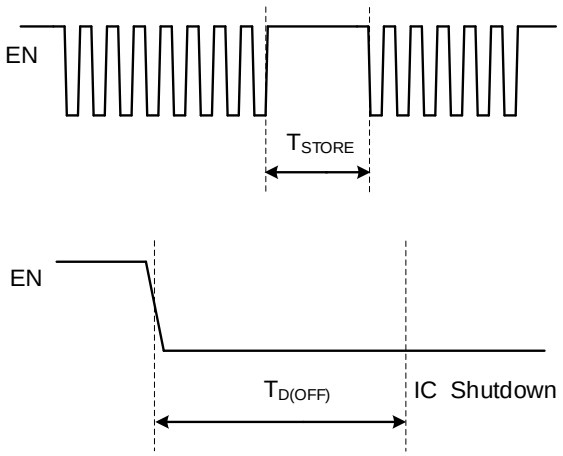


Figure 3. EN digital interface waveform diagram

Protection

The JW7952 guarantees robustness with input over-current protection, thermal shutdown, under voltage lockout and input over voltage protection.

Input Over-Current Protection

The JW7952 measures the inductance peak current by top switchs. And the over-current protection threshold is constant 12.5A.

When the inductance peak current exceeds the input over current threshold, the device turns off the top switches and turns on the bottom switches regardless of the status of PWM1 and PWM2 to protect the chip from damaging. When the over current event happens 4 times, IC will enter hiccup mode.

Under-Voltage Lockout

When the V_{AVIN} falls below the V_{AVIN_UVLO} falling threshold, the device stops switching. When the V_{AVIN} rises above the V_{AVIN_UVLO} rising threshold, the device resumes working, if EN is still high.

Input Over-Voltage Protection

When the V_{PVIN} rises above the V_{PVIN_OVLO} rising threshold, the device stops switching. When the

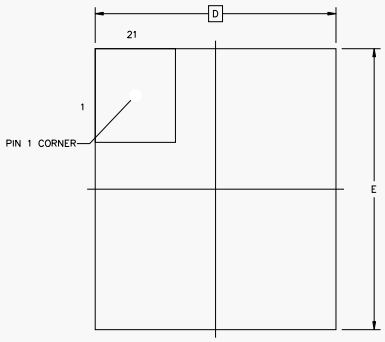
V_{PVIN} falls below the V_{PVIN_OVLO} falling threshold, the device resumes working, if EN is still high and V_{AVIN} is still above the V_{AVIN_UVLO} falling threshold .

Thermal Shutdown

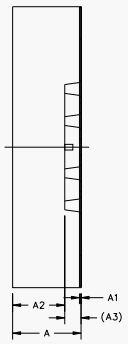
When the junction temperature of the JW7952 rises above 150°C, the device enters shut down mode. When the temperature of JW7952 drops below 130°C, the JW7952 can be resumed.

PACKAGE OUTLINE

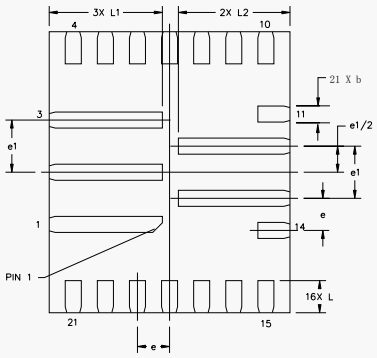
VQFN3x3.5-21 UNIT: mm



TOP VIEW



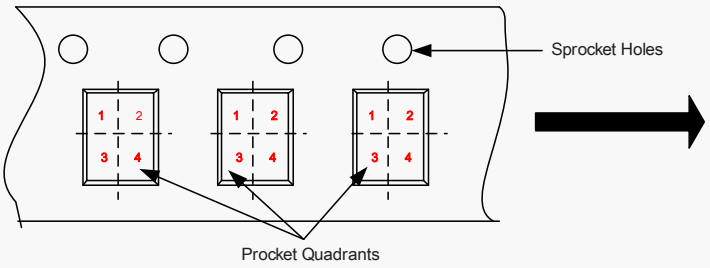
SIDE VIEW



BOTTOM VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.8	0.85	0.9
A1	0	0.02	0.05
A2	——	0.65	——
A3	0.203REF.		
b	0.15	0.2	0.25
D	3.0 BSC		
E	3.5 BSC		
e	0.4 BSC		
e1	0.65 BSC		
L	0.3	0.4	0.5
L1	1.31	1.41	1.51
L2	1.29	1.39	1.49

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPAE



Package Type	Pin1 Quadrant
VQFN3x3.5-21	

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