15W Full-Bridge Power Stage with Voltage/Current Demodulation for Highly-Integrated Wireless Power Transmitter

1 Descriptions

The SC5006 is a highly integrated analog-front-end that contains all of the analog components required to implement a wireless power transmitter compliant with WPC specifications. The device integrates a full-bridge power stage with low-$R_{DS(on)}$ MOSFETs, gate drivers, 5V LDOs, communication demodulators and input current sensing circuit. It can work with a transmitter controller to create a high-performance and cost-effective wireless power transmitter system that complies with WPC QI 1.3.

The wireless power transmitter system supports foreign object detection (FOD) by continuously monitoring the amount of power transferred and comparing it to the amount of received power, as reported by the power receiver. In order to do this, the SC5006 measures the input DC current very accurately using a current sense amplifier. The built-in 5V and 3.3V LDOs can power both the internal and external circuits. Besides, the SC5006 supports under-voltage lockout (UVLO), over-current & short-circuit protection (OCP & SCP) and over-temperature protection (OTP). The protections significantly enhance the reliability of the whole wireless power transmitter system.

The SC5006 is available in a compact 3mm x 3mm QFN package.

2 Features

- WPC QI 1.3 compliant
- Input voltage range: 3V-14V
- Support up to 15W power transfer
- Integrated four 16mohm $R_{DS(on)}$ power MOSFETs
- Integrated FET drivers and bootstrap circuits
- Integrated accurate current sense for FOD
- Integrated voltage and current demodulators
- Integrated Q factor detection
- UVLO/OCP/OTP
- 3mm x 3mm QFN package

3 Applications

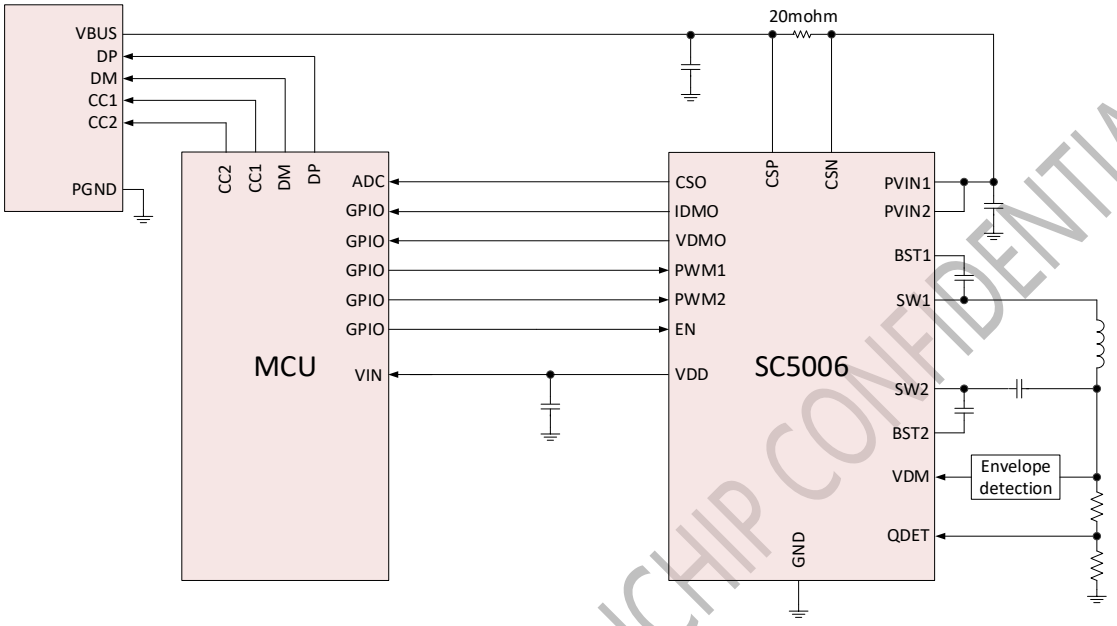
- WPC Compliant Wireless Power Transmitters
- Proprietary Wireless Power Transmitters
- General Wireless Power Chargers for Consumer, Industrial and Medical Applications

4 Device Information

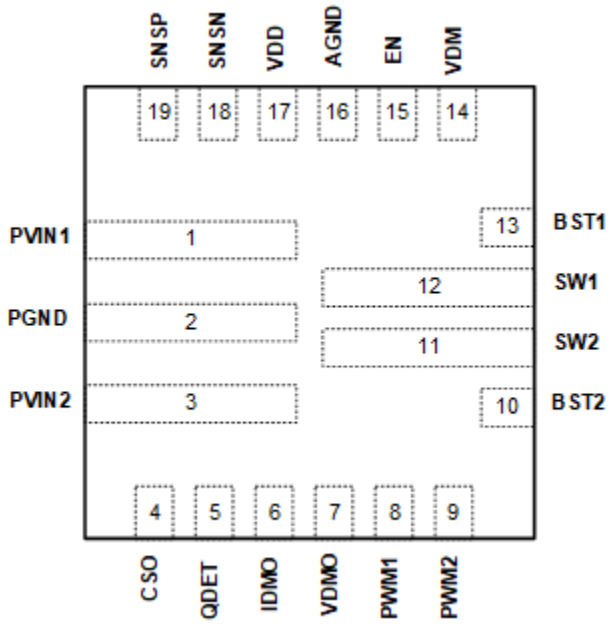
Part Number	Package	Dimension
SC5006	FCQFN3x3_19L	3mm x 3mm x 0.75mm

5 Typical Application Circuit

1) General Wireless Power Transmitter:



6 Terminal Configuration and Functions



SC5006 (Top View) FCQFN3x3_19L

TERMINAL		I/O	DESCRIPTION
NUMBER	NAME		
1	PVIN1	I	Input voltage for half-bridge MOSFET. Bypass with a 10 µF ceramic capacitor to PGND.
2	PGND	PWR	Power ground.
3	PVIN2	I	Input voltage for half-bridge MOSFET. Bypass with a 22 µF ceramic capacitor to PGND.
4	CSO	O	Current sense amplifier output.
5	QDET	I	Q factor detect pin.
6	IDMO	O	Output of the demodulated 2-kHz communication signal based on current demodulation scheme.
7	VDMO	O	Output of the demodulated 2-kHz communication signal based on voltage demodulation scheme.
8	PWM1	I	PWM logic input for the Q1 and Q2 as shown in the Block Diagram. Logic HIGH turns on the high-side FET Q1, and turns off the low-side FET Q2. Logic LOW turns on the low-side FET Q2 and turns off the high-side FET Q1
9	PWM2	I	PWM logic input for the Q3 and Q4 as shown in the Block Diagram. Logic HIGH turns on the high-side FET Q3, and turns off the low-side FET Q4. Logic LOW turns on the low-side FET Q4 and turns off the high-side FET Q3
10	BST2	I/O	Connect a 0.1 µF capacitor between BST2 and SW2 to bootstrap a voltage to provide the bias for high side MOSFET driver.
11	SW2	O	Switch node of the half-bridge MOSFET.
12	SW1	O	Switch node of the half-bridge MOSFET.
13	BST1	I/O	Connect a 0.1 µF capacitor between BST1 and SW1 to bootstrap a voltage to provide the bias for high side MOSFET driver.
14	VDM	I	High-pass filter input. Voltage demodulation pin for data packets based on coil voltage variation.
15	EN	I	Enable pin. Logic LOW disables the IC. Logic HIGH enables the IC. Use pulse signal communication at EN pin.
16	AGND	O	AGND pin.
17	VDD	O	Output of internal regulator to provide 5.0V power supply to internal gate drivers and control circuits. Connect a 2.2 µF ceramic capacitor from VDD to AGND pin.
18	CSN	I	Negative end of input current sense amplifier.
19	CSP	I	Positive end of input current sense amplifier.

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Voltage range at terminals (2)	PVIN1, PVIN2, SW1, SW2, CSP, CSN	-0.3	16.5	V
	PWM1, PWM2, EN, CSO, VDM, VDMO, IDMO, VDD	-0.3	6.5	V
	BST1, BST2	-0.3	21.5	V
	QDET	-0.3	30	V
Differential Voltage range between terminals	CSP-CSN	-0.6	0.6	V
Temperature Range	Operating Junction, T_J	-40	150	°C
	Storage temperature range, T_{stg}	-65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

7.2 Thermal Information

THERMAL RESISTANCE(1)		QFN-19 (3mm x 4mm)	UNIT
Θ_{JA}	Junction to ambient thermal resistance	47	°C/W
Θ_{JC}	Junction to case resistance	13	°C/W

(1) Measured on JESD51-7, 4-layer PCB.

7.3 Handling Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
ESD (1)	Human body model (HBM) ESD stress voltage(2)	-2000	2000	V
	Charged device model (CDM) ESD stress voltage (3)	-750	750	V

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.

(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.4 Recommended Operating Conditions

		MIN	TYP	MAX	UNIT
V_{PVIN1}, V_{PVIN2}	Input voltage range	3		14	V
C_{PVIN1}, C_{PVIN2}	PVIN1, PVIN2 Ceramic Capacitor		22		µF
C_{BST1}, C_{BST2}	BST1-SW1, BST2-SW2 Ceramic Capacitor		0.1		µF
C_{VDD}, C_{V3P3}	VDD, V3P3 Ceramic Capacitor		2.2		µF

T_J	Operating junction temperature	-40		125	°C

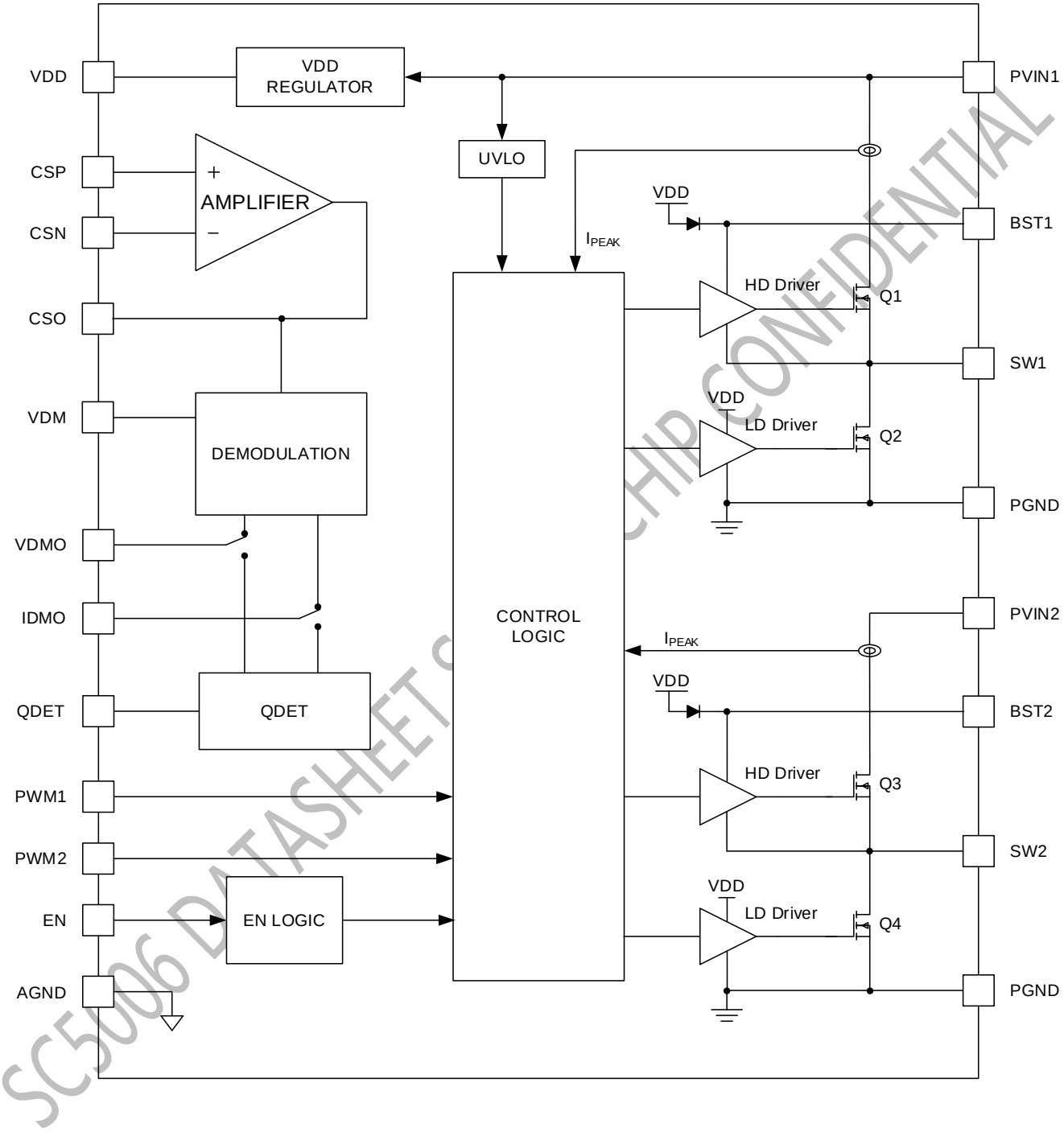
7.5 Electrical Characteristic

V_{PVIN1} = V_{PVIN2} = 12V, typical values are tested at room temperature, unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
V_{PVIN}	Operating input voltage		3		14	V
V_{IN_UVLO}	Under voltage lockout threshold	Rising edge		2.8		V
		Falling edge		2.6		V
I_Q	Quiescent current into PVIN	EN= high, no switching, V_{PVIN}=12V		1.25		mA
I_{Q_SLEEP}	Quiescent current into PVIN	EN=high, enter sleep mode, V_{PVIN}=3.5V		40		μA
I_{SD}	Shutdown current into PVIN	EN =low, V_{PVIN}=3.5V		5		μA
VOLTAGE REGULATOR (VDD)						
V_{DD_5V}	VDD output voltage, VDD set to 5V	V_{PVIN} = 5V, Cout = 2.2μF		4.8		V
		V_{PVIN} = 12V, Cout = 2.2μF	4.85	5	5.15	V
V_{DD_4P5V}	VDD output voltage, VDD set to 4.5V	V_{PVIN} = 5V&12V, Cout = 2.2μF	4.3	4.5	4.7	V
I_{VDD_LIM}	VDD output current capability	V_{PVIN}≥5V, Cout = 2.2uF	70			mA
CURRENT SENSE AMPLIFIER						
I_{PVIN}	Input current range	Sense Resistor=20mohm, VDD = 5.0V	0		3.5	A
G	Gain	Sense Resistor=20mohm, Sense Current=2A	0.98	1	1.02	V/A
V_{CSO0}	CSO offset voltage	Measured at the CSO pin; V_{CSP} = V_{CSN}		0.5		V
POWER SWITCH						
$R_{DS(on)}$	SW1 High-side $R_{DS(on)}$	V_{DD} = 5.0V		16		mΩ
	SW1 Low-side $R_{DS(on)}$	V_{DD} = 5.0V		16		mΩ
	SW2 High-side $R_{DS(on)}$	V_{DD} = 5.0V		16		mΩ
	SW2 Low-side $R_{DS(on)}$	V_{DD} = 5.0V		16		mΩ
OVER CIRCUIT PROTECTION						
I_{LIM}	High-side current limit threshold			10		A
T_p	Hiccup period			20		ms
CNT_{OCP}	OCP deglitch count			4		
EN, PWM1, PWM2						
V_{IH}	Input logic high				2.65	V
V_{IL}	Input logic low		0.65			V
VDMO, IDMO						
V_{OH}	Output logic high		0.9*VDD			V
V_{OL}	Output logic low				0.1	V

THERMAL SHUTDOWN				
T_{SD}	Thermal shutdown temperature		160	°C
	Thermal shutdown hysteresis		25	°C

8 Functional Block Diagram



9 Feature Description

9.1 Enable and Start up Logic

The UVLO function protects the chip from operating at insufficient power supply. When the input voltage rises above 3V and the EN pin voltage exceeds the high threshold of 2.65V, the 5V voltage regulator works at once, It should be noted that the EN pin is pulled up internally in the chip. Once the PVIN and VDD voltage exceed their own high threshold, the full-bridge power stage responses to the PWM logic.

When the EN pin is pulled down externally, the chip is disabled, and the shutdown current into PVIN pins is about 12uA (typical).

9.2 Current Sense Amplifier

To support foreign object detection (FOD), the SC5006 senses the input average current by means of external resistor and internal amplifier. The integrated current sense amplifier has a typical voltage gain of 50. For proper scaling of the current signal, the recommended current sense resistor is 10mΩ/20mΩ.

The current sense amplifier output has a typical 0.5V offset voltage when the sensed current is zero. For accurate measurement of the input current, MCU need to calibrate this offset.

9.3 PWM Control

The PWM1 input controls the internal MOSFETs Q1 and Q2, and the PWM2 input controls the internal MOSFETs Q3 and Q4 as shown in the Block Diagram. The PWM1 and PWM2 can independently control the SW1 and SW2 duty cycle and frequency. Please be noted that the dead time has already been implemented between Q1 (or Q3) and Q2 (or Q4) internally, so there is no need for dead time between external control signals PWM1 and PWM2.

9.4 Voltage Regulators

The SC5006 has integrated 5V voltage regulators to power internal gate drivers, control circuits and external transmitter controller. The 5V voltage regulator is powered from PVIN and supplies a regulated 5V voltage at the VDD pin. Decouple the VDD pin with 2.2μF low-ESR ceramic capacitors that are placed close to the IC. The load capability of 5V regulators is about 100mA respectively.

9.5 Voltage Demodulation

In order to increase the communication reliability in any load condition, the SC5006 has integrated two demodulation schemes, one based on input peak current information and the other based on coil voltage information. The voltage mode envelope detector is implemented using a discrete solution as depicted in Figure 1. This simple implementation achieves the envelope detector function as well as the DC filter function.

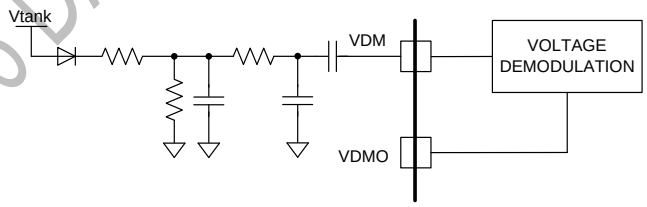


Fig1. Voltage Demodulation

9.6 Current Demodulation

The current-mode detector takes the modulation information from the input peak current as depicted in Figure 2. The MCU can detect the demodulation results on VDMO and IDMO pins and then implement the packet decode. It can select either voltage-mode or current-mode signals depending upon which produces the best demodulated signal.

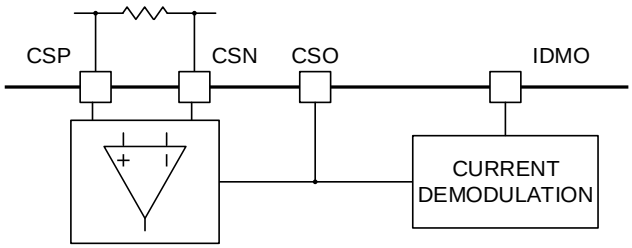


Fig2. Current Demodulation

9.7 Over-Current Protection (OCP)

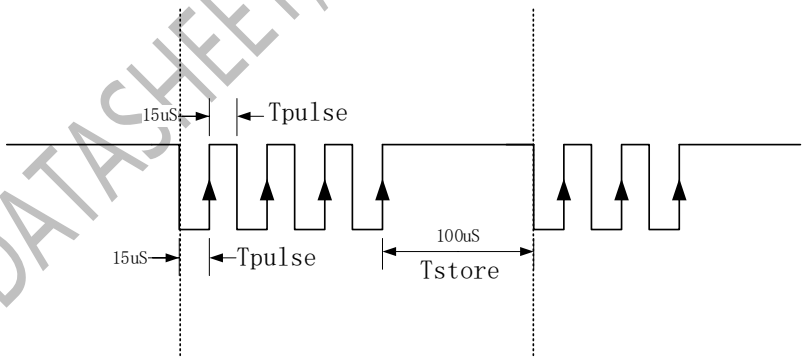
The SC5006 integrates hiccup-mode-based over-current protection. The currents of the SW1 high-side FET and SW2 high-side FET are sensed and compared to the current-limit threshold during every switching cycle. When the sensed current reaches the current-limit threshold, the over-current fault counter is incremented. If the over-current fault counter reaches 4 and overflows, the high side FETs are turned off and the low side FETs are turned on regardless of the PWM inputs. The IC remains in the hiccup mode for a period equal to 10ms typically and then attempts to restart. The hiccup mode OCP protection can reduce the average current greatly to alleviate the thermal issue and to protect the chip. Once the OCP condition is removed, the SC5006 exits hiccup mode and goes back to normal operation.

9.8 Over Temperature Protection (OTP)

The over temperature protection (OTP) prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 160℃, the SC5006 is shut down. When the temperature drops below threshold (typically 135℃), the chip is enabled again.

9.9 Digital Interface(EN Pin)

SC5006 includes a digital interface that can control the internal function block of the chip. The EN timing is shown in the figure below.



Figue3

The digital interface is controlled by counting the number of rising edges on the EN pin, Pulse timing as the figure3, The pulse interval is Tpulse (15uS). After the pulse configuration is completed, the EN pin is high level than Tstore (100uS) , the configuration effective.

The number of rising edges and configured as shown below.

Rising Edges	Function
3	IDMO input select I average
4	Enable Q factor detection
0/5	Disable Q factor detection
0/6	Q factor detection comp Vth high to 400mV
7	Q factor detection comp Vth high to 200mV
0/8	Q factor detection comp Vth low to 100mV
9	Q factor detection comp Vth low to 50mV
10	VDD output select 4P5V
11	Enter Sleep mode
12	Dead time = 100nS
0/13	Dead time = 200nS
14	Dead time = 20nS
15	Dead time = 40nS
16	Driver speed slowest
17	Driver speed slow
0/18	Driver speed fast
19	Driver speed fastest
25	VDM gain select 4

10 Application Information

10.1 Input Current Sense

The SC5006 senses the input average current accurately for foreign object detection. The recommended current sense resistance is 10mΩ/20mΩ. Resistor of 1% or higher accuracy and low temperature coefficient is recommended.

The resistor power rating and temperature coefficient should also be considered. The power dissipation is roughly calculated as $P=I^2R$, and I is the highest current flowing through the resistor. The resistor power rating should be higher than the calculated value.

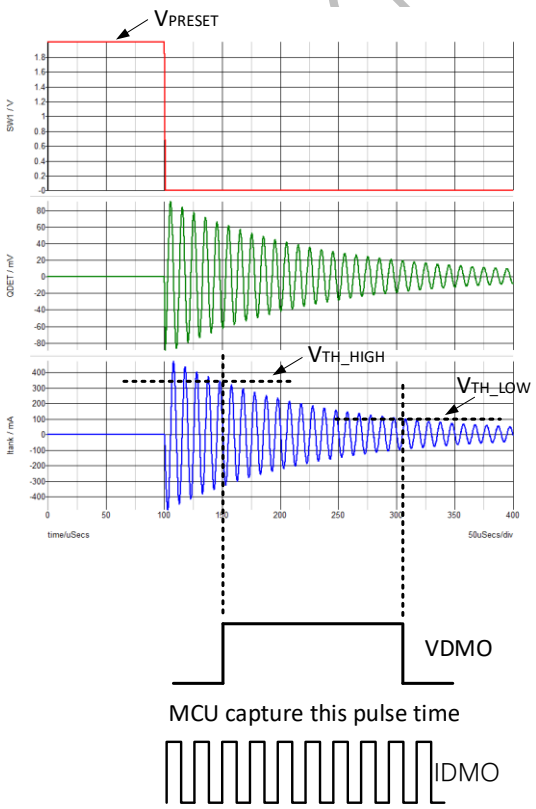
The current sense amplifier output has a typical 0.5V offset when the sensed current is zero. Please be noted that this offset may vary a little from one chip to another, so when MCU is calibrating this offset, it is highly recommended to use ADC to sense this offset instead of using fixed 0.5V.

10.2 Voltage and Current Demodulation

The SC5006 simultaneously integrates voltage and current demodulation which are based on coil peak voltage and input peak current separately. Compared with the discrete demodulation solution, the chip need much less number of external components.

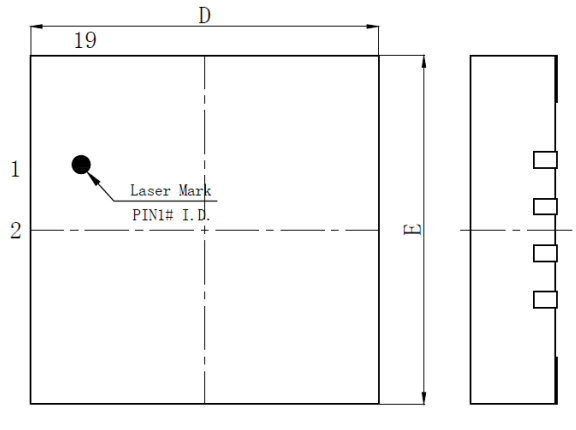
10.3 Q detect

SC5006 Integrated Q-detect function, Q-detect can be controlled through the EN digital interface.

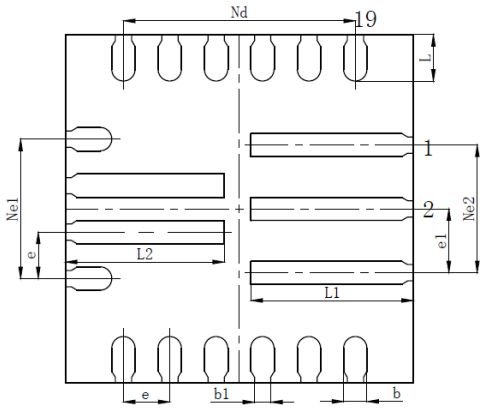


11 MECHANICAL DATA

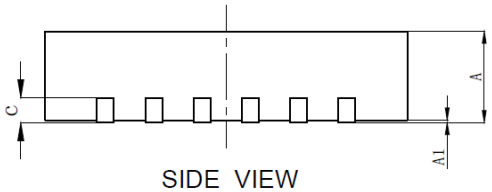
FCQFN19 (3x3x0.75)



TOP VIEW



BOTTOM VIEW



SIDE VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.15	0.20	0.25
b1	0.14REF		
c	0.203REF		
D	2.90	3.00	3.10
e	0.40BSC		
e1	0.55BSC		
Ne1	1.20BSC		
Ne2	1.10BSC		
Nd	2.00BSC		
E	2.90	3.00	3.10
L	0.35	0.40	0.45
L1	1.35	1.40	1.45
L2	1.32	1.37	1.42