N-channel MOSFET

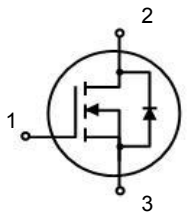
Features

- High ruggedness
- $R_{DS(ON)}$ (Max 3.15Ω)@V_{GS}=10V
- Fast reverse recovery body diode
- Improved dv/dt Capability
- 100% Avalanche Tested

BV_{DSS} : 500V
I_D : 3A
$R_{DS(ON)}$: 2.70ohm

TO-252

1. Gate 2. Drain 3. Source



General Description

This power MOSFET is produced with advanced VDMOS technology.
This technology enable power MOSFET to have better characteristics, such as fast switching time, low on resistance, low gate charge and especially excellent avalanche characteristics. It is mainly suitable for half bridge or full bridge resonant topology like a electronic ballast, and also low power switching mode power appliances.

Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DSS}	Drain to Source Voltage	500	V
I_D	Continuous Drain Current (@T_c=25°C)	3.0	A
	Continuous Drain Current (@T_c=100°C)	1.9	A
I_{DM}	Drain current pulsed (note 1)	9.0	A
V_{GS}	Gate to Source Voltage	± 30	V
E_{AS}	Single pulsed Avalanche Energy (note 2)	120	mJ
E_{AR}	Repetitive Avalanche Energy (note 1)	8.9	mJ
dv/dt	Peak diode Recovery dv/dt (note 3)	4.5	V/ns
P_D	Total power dissipation (@T_C=25°C)	79	W
	Derating Factor above 25°C	0.75	W/°C
T_{STG} , T_J	Operating Junction Temperature & Storage Temperature	-55 ~ + 150	°C
T_L	Maximum Lead Temperature for soldering purpose, 1/8 from Case for 5 seconds.	300	°C

Thermal characteristics

Symbol	Parameter	Value	Unit
R_{thjc}	Thermal resistance, Junction to case	1.57	°C/W
R_{thja}	Thermal resistance, Junction to ambient	110	°C/W

Electrical characteristic (T_C = 25°C unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Off characteristics						
BV_{DSS}	Drain to source breakdown voltage	V_{GS}=0V, I_D=250uA	500	-	-	V
ΔBV_{DSS} / ΔT_J	Breakdown voltage temperature coefficient	I_D=250uA, referenced to 25°C	-	0.64	-	V/°C
I_{DSS}	Drain to source leakage current	V_{DS}=500V, V_{GS}=0V	-	-	1	uA
		V_{DS}=400V, T_C=125°C	-	-	10	uA
I_{GSS}	Gate to source leakage current, forward	V_{GS}=30V, V_{DS}=0V	-	-	100	nA
	Gate to source leakage current, reverse	V_{GS}=-30V, V_{DS}=0V	-	-	-100	nA
On characteristics						
$V_{GS(TH)}$	Gate threshold voltage	V_{DS}=V_{GS}, I_D=250uA	2.5	-	4.5	V
$R_{DS(ON)}$	Drain to source on state resistance	V_{GS}=10V, I_D = 1.50A		2.70	3.15	Ω
Dynamic characteristics						
C_{iss}	Input capacitance	V_{GS}=0V, V_{DS}=25V, f=1MHz			680	pF
C_{oss}	Output capacitance				91	
C_{rss}	Reverse transfer capacitance				13	
$t_{d(on)}$	Turn on delay time	V_{DS}=250V, I_D=3.0A, R_G=25Ω			33	ns
tr	Rising time				41	
$t_{d(off)}$	Turn off delay time				174	
t_f	Fall time				42	
Q_g	Total gate charge	V_{DS}=400V, V_{GS}=10V, I_D=3.0A		10	13	nC
Q_{gs}	Gate-source charge			1.7		
Q_{gd}	Gate-drain charge			5		

Source to drain diode ratings characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_S	Continuous source current	Integral reverse p-n Junction diode in the MOSFET	-	-	3.0	A
I_{SM}	Pulsed source current		-	-	11	A
V_{SD}	Diode forward voltage drop.	I_S=3.0A, V_{GS}=0V	-	0.9	1.4	V
T_{rr}	Reverse recovery time	I_S=3.0A, V_{GS}=0V, dIF/dt=100A/us	-	60	-	ns
Q_{rr}	Breakdown voltage temperature		-	0.5	-	uC

※. Notes
1. Repeatitive rating : pulse width limited by junction temperature.
2. L = 25mH, I_{AS} = 3.0A, V_{DD} = 50V, R_G=50Ω, Starting T_J = 25°C
3. I_{SD} ≤ 3.0A, di/dt = 300A/us, V_{DD} ≤ BV_{DSS}, Staring T_J =25°C
4. Pulse Test : Pulse Width ≤ 300us, duty cycle ≤ 2%
5. Essentially independent of operating temperature.

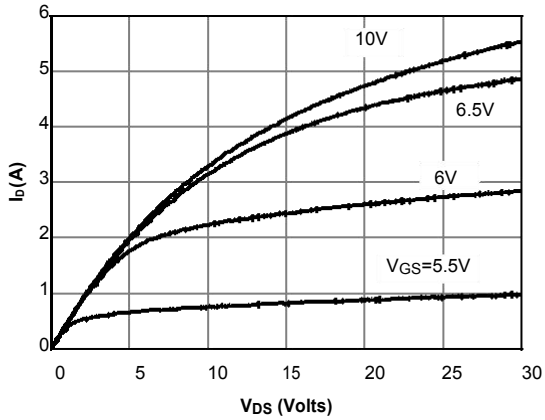


Fig 1: On-Region Characteristics

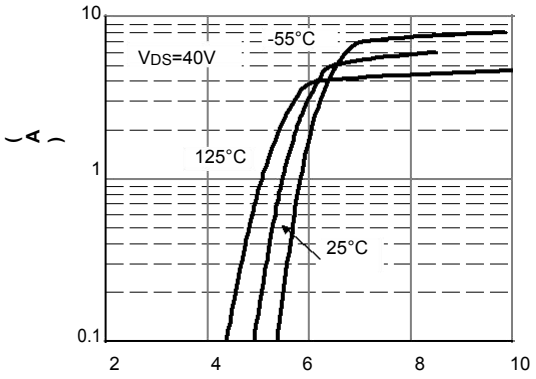


Figure 2: Transfer Characteristics

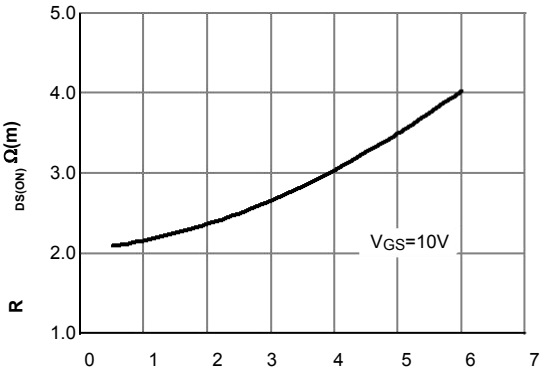


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

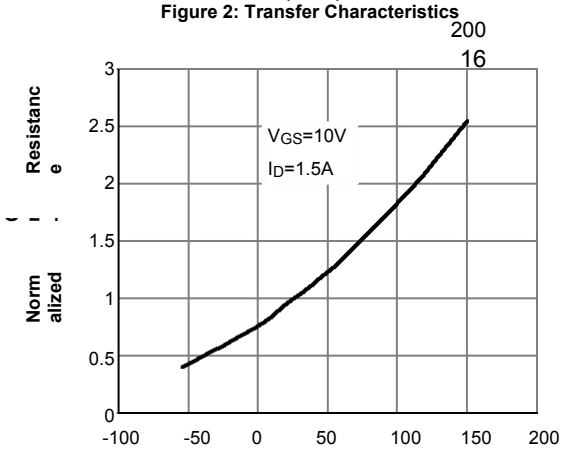


Figure 4: On-Resistance vs. Junction Temperature

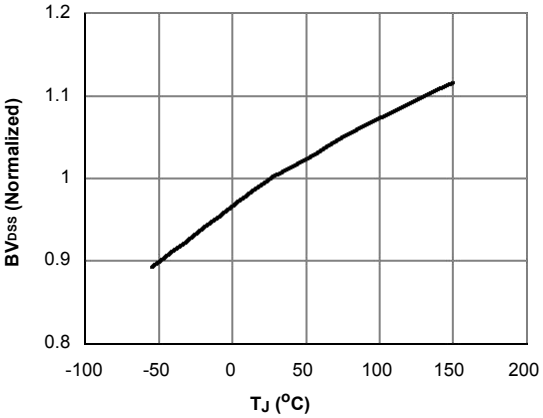


Figure 5: Break Down vs. Junction Temperature

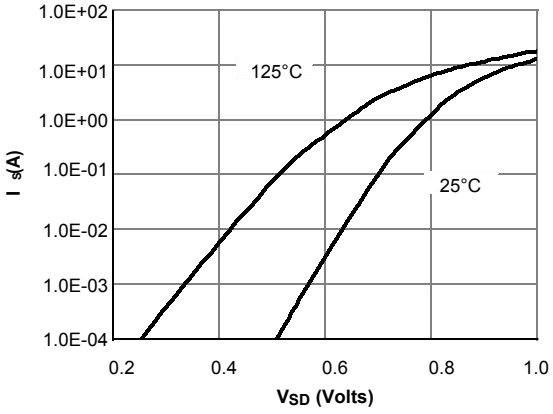


Figure 6: Body-Diode Characteristics

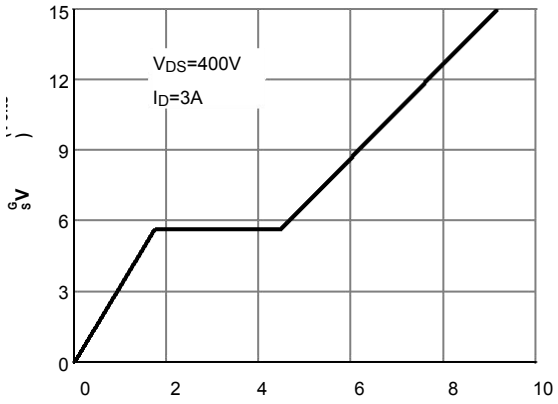


Figure 7: Gate-Charge Characteristics

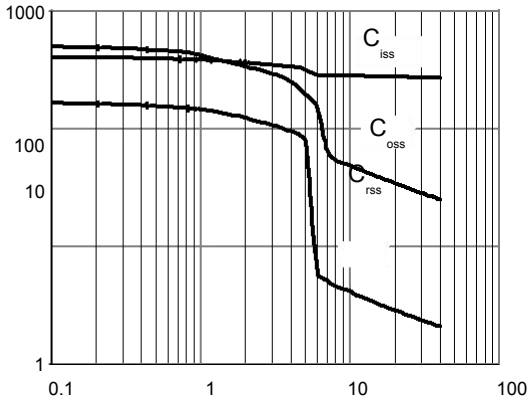


Figure 8: Capacitance Characteristics

200

16

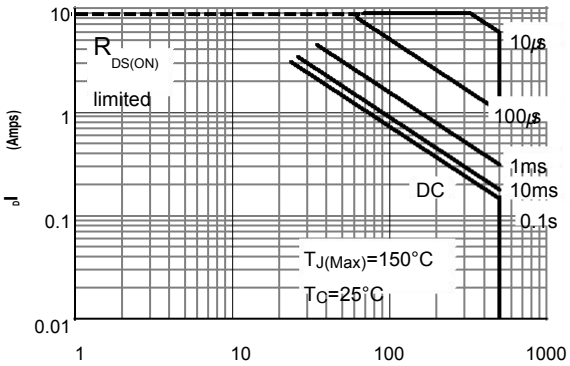


Figure 9: Maximum Forward Biased Safe Operating Area for AOT3N50 (Note F)

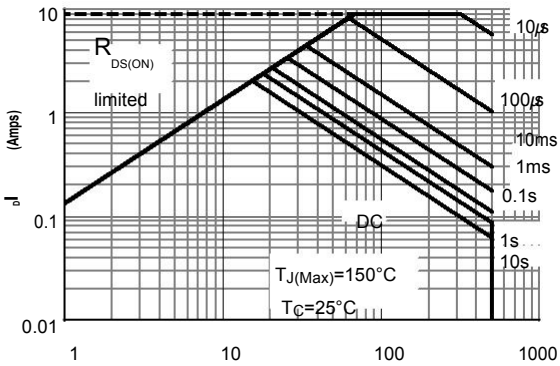


Figure 10: Maximum Forward Biased Safe Operating Area for AOTF3N50 (Note F)

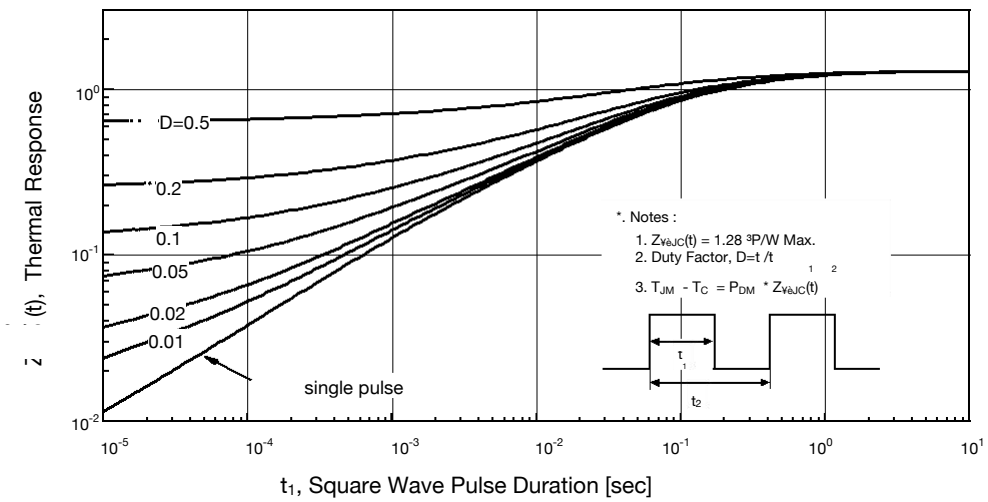


Fig. 11. Transient thermal response curve

Fig. 12. Gate charge test circuit & waveform

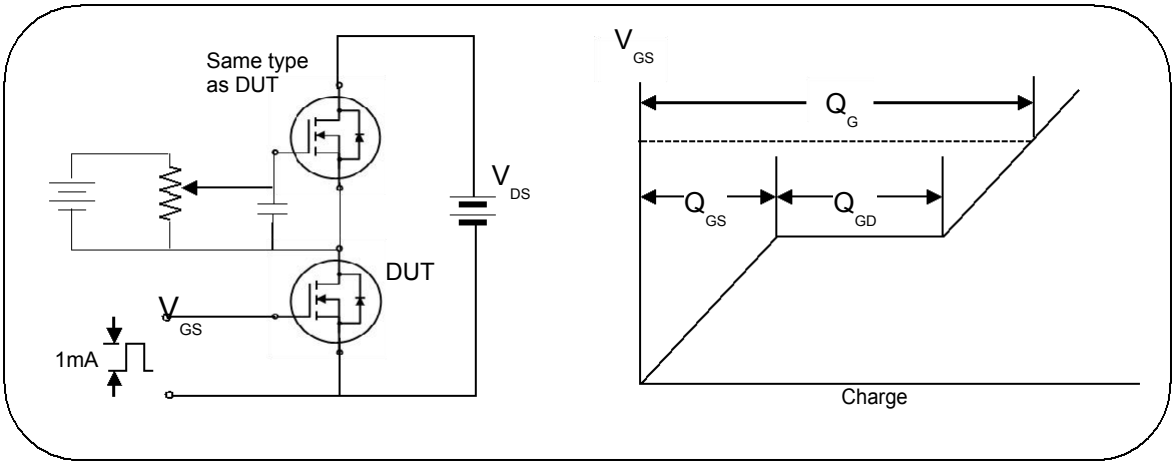


Fig. 13. Switching time test circuit & waveform

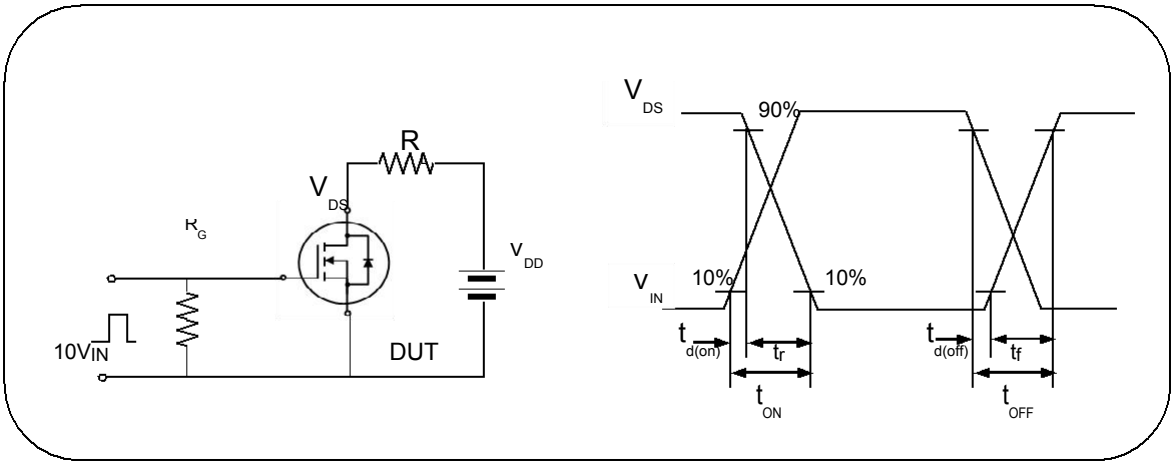


Fig. 14. Unclamped Inductive switching test circuit & waveform

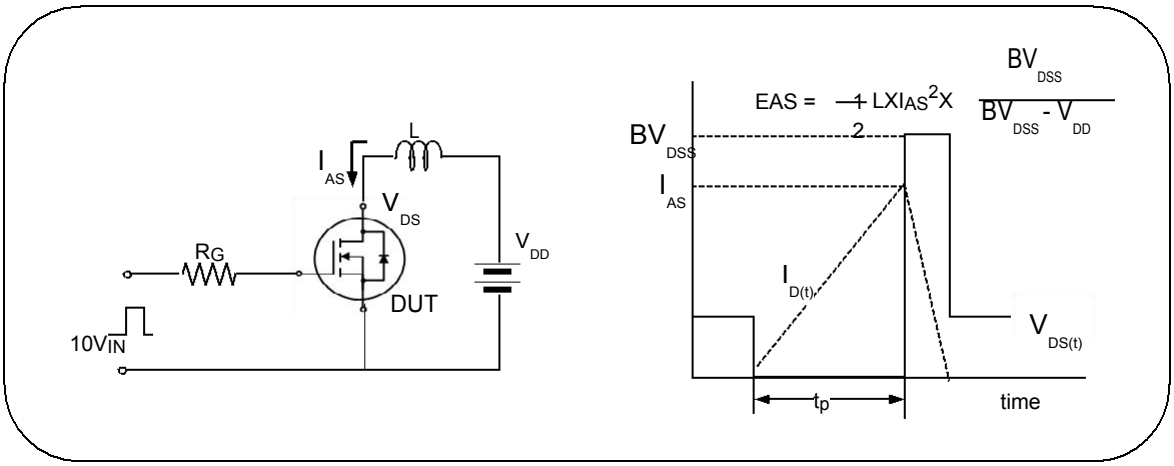


Fig. 15. Peak diode recovery dv/dt test circuit & waveform