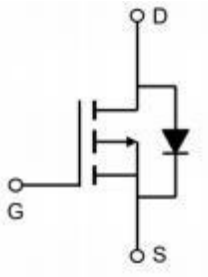
CP20P01BF

-18V P-Channel Enhancement Mode MOSFET

Description

The CP20P01BF uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a Battery protection or in other Switching application.

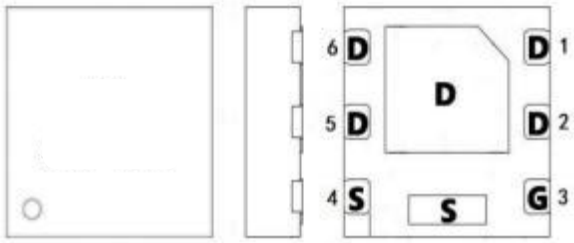


General Features

V_{DS} = -18V I_D =-20A

$R_{DS(ON)}$ < 18mΩ @ V_{GS}=10V **（Type：12mΩ）**

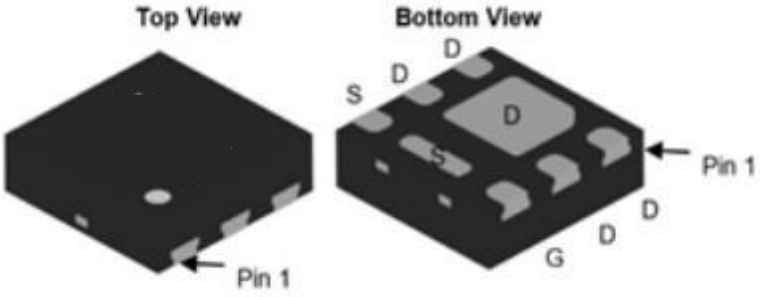
$R_{DS(ON)}$ < 23mΩ @ V_{GS}=4.5V **（Type：14mΩ）**



Application

Electronic cigarette

Load switch



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
CP20P01BF	QFN2*2-6L	CP20P01BF XXX YYYY	3000

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Symbol	Parameter	Rating	Units
VDSS	Drain-Source Voltage	-18	V
VGSS	Gate-Source Voltage	±12	V
I_D@T_C=25℃	Continuous Drain Current, V_{GS} @ 10V[1]	-20	A
I_D@T_C=100℃	Continuous Drain Current, V_{GS} @ 10V[1]	-10.6	A
IDM	Pulsed Drain Current note1	-36	A
P_D@T_C=25℃	Power Dissipation	1.6	W
RθJA	Thermal Resistance, Junction to Ambient	125	℃/W
TJ, TSTG	Operating and Storage Temperature Range	-55 to +150	℃

Electrical Characteristics (T_J=25℃, unless otherwise noted)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V(BR)DSS	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=-250μA	-12	-18	-	V
IDSS	Zero Gate Voltage Drain Current	V_{DS} =-12V, V_{GS} = 0V,	-	-	-1	μA
IGSS	Gate to Body Leakage Current	V_{DS} =0V, V_{GS} = ±12V	-	-	±100	nA
VGS(th)	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=-250μA	-0.5	-0.65	-1.0	V
RDS(on)	Static Drain-Source on-Resistance note2	V_{GS}=-10V, I_D =-6.0A	-	12	18	mΩ
RDS(on)	Static Drain-Source on-Resistance note2	V_{GS}=-4.5V, I_D=-5.2A	-	14	23	mΩ
RDS(on)	Static Drain-Source on-Resistance note2	V_{GS}=-2.5V, I_D=-4.2A		20	35	mΩ
C_{iss}	Input Capacitance	V_{DS}=-6V, V_{GS}=0V f=1.0MHz	-	1100	-	pF
Coss	Output Capacitance		-	390	-	pF
Crss	Reverse Transfer Capacitance		-	300	-	pF
Q_g	Total Gate Charge	V_{DS}=-4V, I_D=-4.1A, V_{GS} = -4.5V	-	11.5		nC
Q_{gs}	Gate-Source Charge		-	1.5	-	nC
Q_{gd}	Gate-Drain(“Miller”) Charge		-	3.2	-	nC
td(on)	Turn-on Delay Time	V_{DD} =-4V, I_D=-3.3A, R_G=1.0Ω, V_{GEN}=-4.5V, R_L=1.2Ω	-	25	-	ns
t_r	Turn-on Rise Time		-	45	-	ns
td(off)	Turn-off Delay Time		-	72	-	ns
t_f	Turn-off Fall Time		-	60	-	ns
IS	Maximum Continuous Drain to Source Diode Forward Current		-	-	-6.0	A
ISM	Maximum Pulsed Drain to Source Diode Forward Current		-	-	-16	A
VSD	Drain to Source Diode Forward Voltage	V_{GS}=0V, I_S =-4.1A	-	-	-1.2	V
t_{rr}	Reverse Recovery Time	V_{GS}=0V, I_S=-4.1A, di/dt=100A/μs	-	20	-	ns
Q_{rr}	Reverse Recovery Charge		-	9	-	nC

Note：

1、The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.

2、The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%

3、The power dissipation is limited by 150℃ junction temperature

4、The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Characteristics

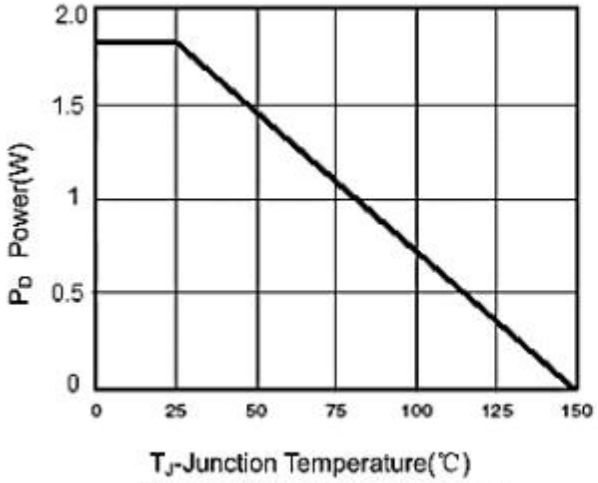


Figure 1 Power Dissipation

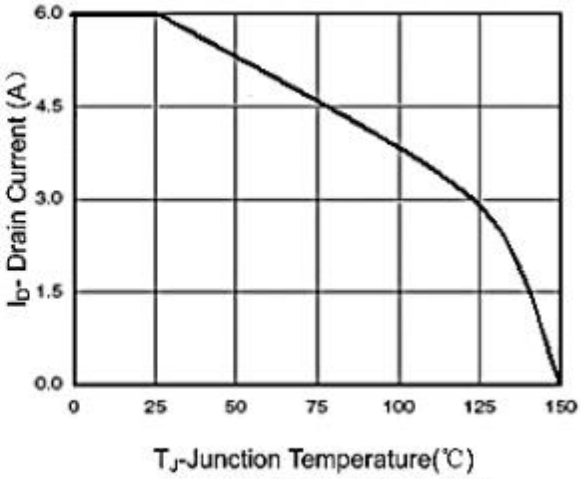


Figure 2 Drain Current

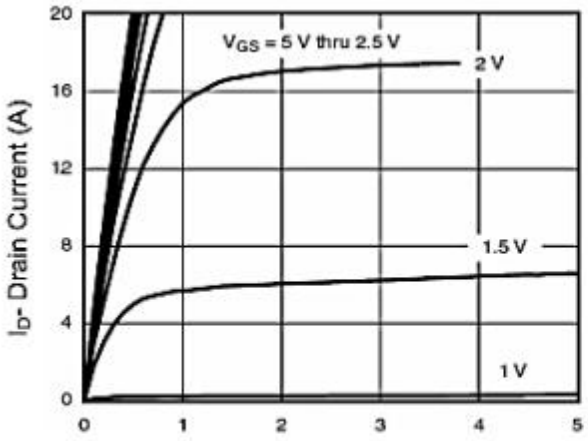


Figure 3 Output Characteristics

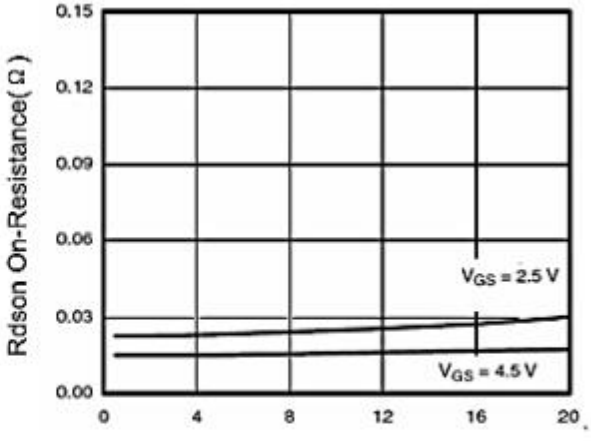


Figure 4 Drain-Source On-Resistance

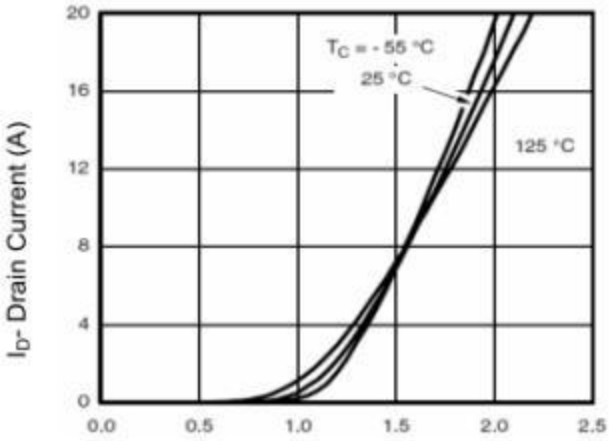


Figure 5 Transfer Characteristics

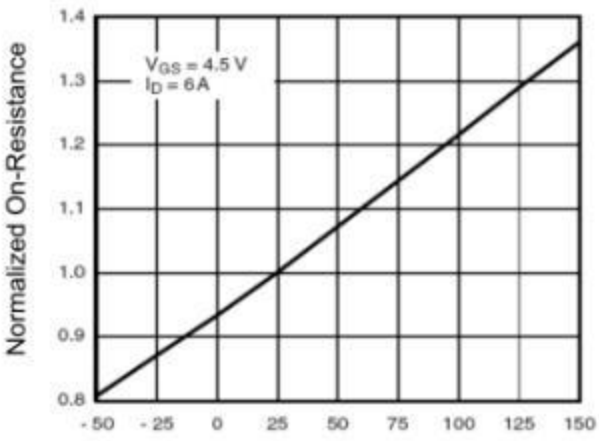


Figure 6 Drain-Source On-Resistance

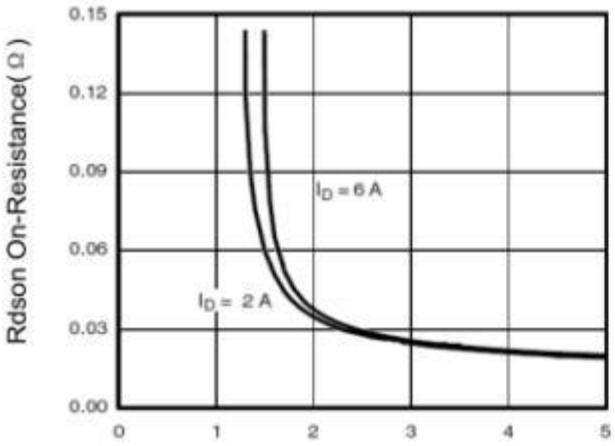


Figure 7 Rdson vs Vgs

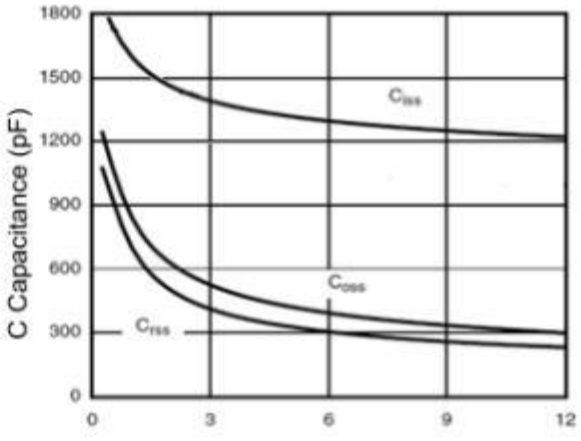


Figure 8 Capacitance vs Vds

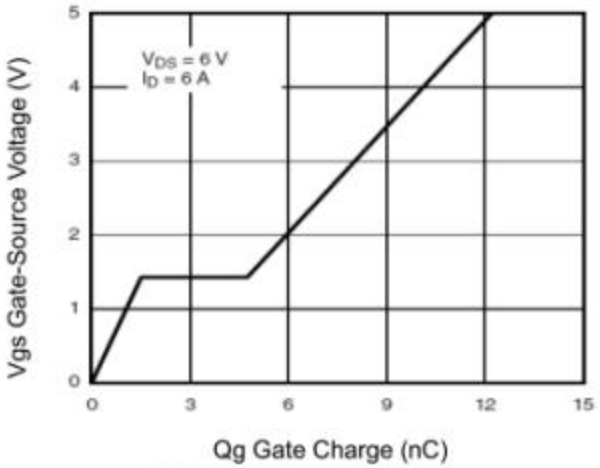


Figure 9 Gate Charge

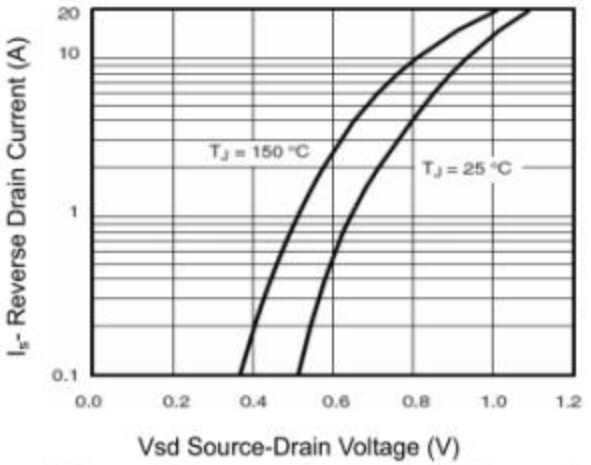


Figure 10 Source- Drain Diode Forward

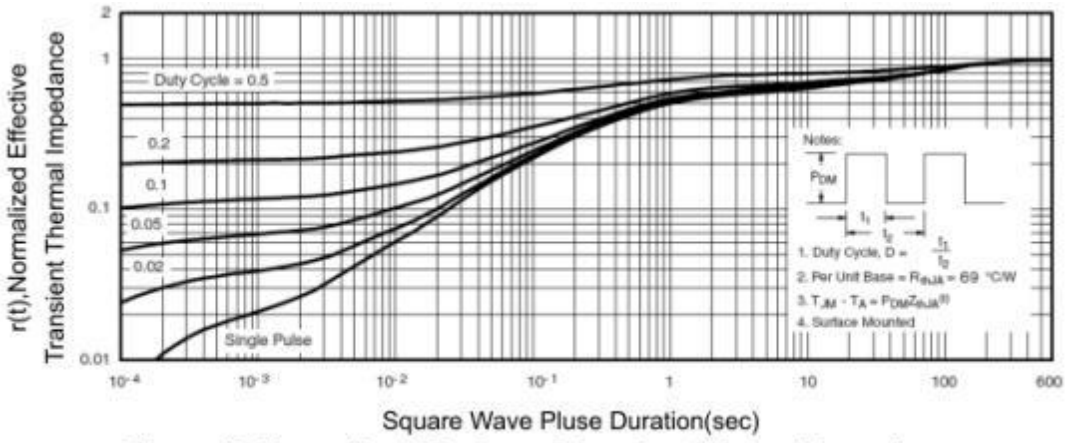
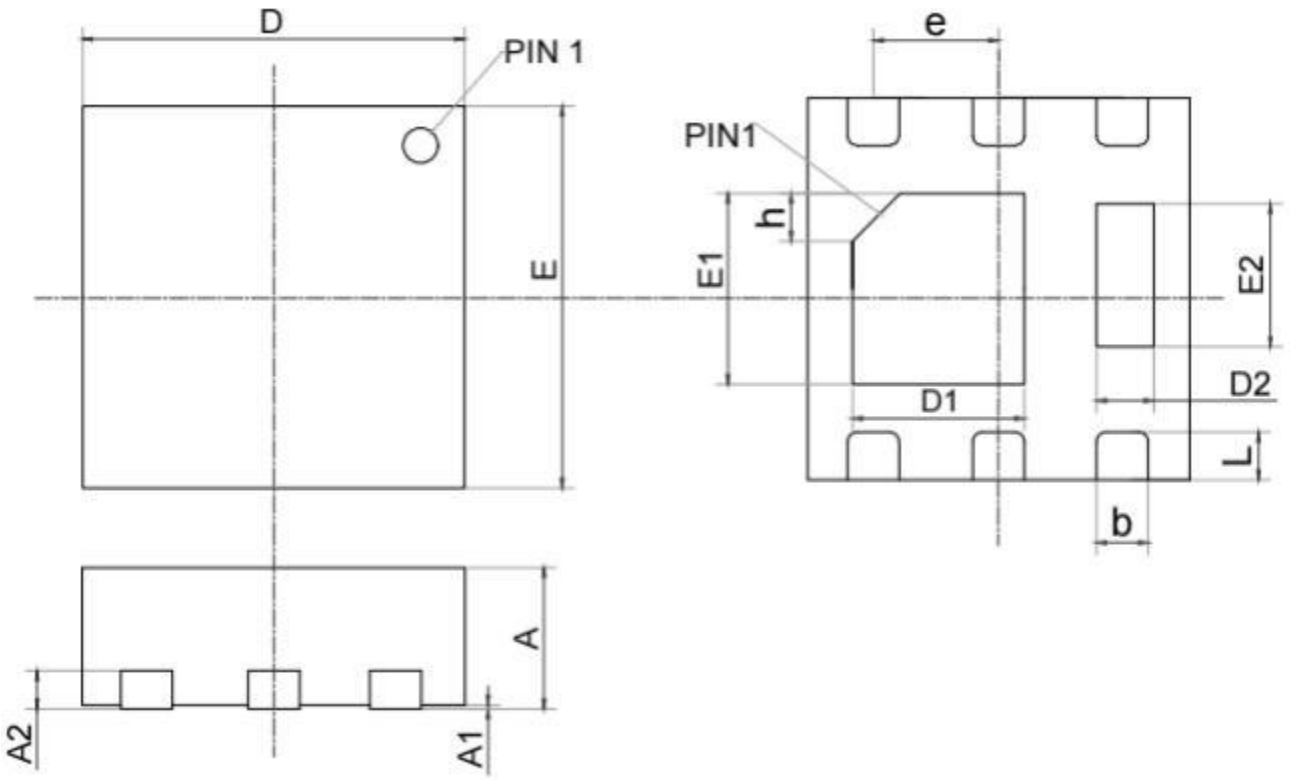


Figure 12 Normalized Maximum Transient Thermal Impedance

Package Mechanical Data：QFN2*2-6L



Symbol			
	Min	Nom	Max
A	0.70	0.75	0.80
A1	--	0.02	0.05
A2	0.18	0.20	0.25
b	0.20	0.27	0.34
D	1.95	2.00	2.05
E	1.95	2.00	2.05
D1	0.80	0.90	1.00
E1	0.90	1.00	1.10
D2	0.20	0.30	0.40
E2	0.65	0.75	0.85
L	0.20	0.25	0.35
h	0.20	0.25	0.30
e	0.65 BSC		

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-18V P-Channel Enhancement Mode MOSFET

Edition	Date	Change
Rve1.0	2020/9/8	Initial release