

40V N-Channel Enhancement Mode MOSFET

Description

The CP40N04QR uses Trench technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of $R_{DS(ON)}$ and Q_g . This device is ideal for high-frequency switching and synchronous rectification.

General Features

- ◆ $V_{DS} = 40V$, $I_D = 40A$
 $R_{DS(ON)} = 6.6m\Omega$ (typical) @ $V_{GS} = 10V$
 $R_{DS(ON)} = 9m\Omega$ (typical) @ $V_{GS} = 4.5V$
- ◆ Excellent gate charge x $R_{DS(ON)}$ product(FOM)
- ◆ Very low on-resistance $R_{DS(ON)}$
- ◆ 150 °C operating temperature
- ◆ Pb-free lead plating
- ◆ 100% UIS tested

Application

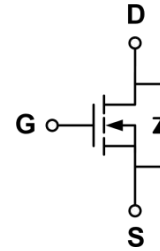
- ◆ DC/DC Converter
- ◆ Ideal for high-frequency switching and synchronous rectification

Package

- ◆ DFN3X3-8L



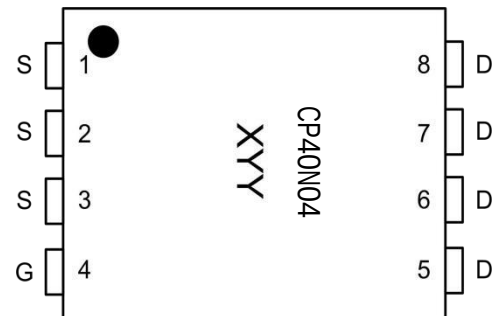
Schematic diagram



Marking and pin assignment

DFN3×3-8L

(Top View)



XXXX—Wafer Information

YYYY—Quality Code

Ordering Information

Part Number	Storage Temperature	Package	Devices Per Reel
CP40N04QR-G	-55°C to +150°C	DFN3X3-8L	5000

Absolute Maximum Ratings (TA=25°C unless otherwise noted)

parameter	symbol	limit	unit
Drain-source voltage	V_{DS}	40	V
Gate-source voltage	V_{GS}	±20	V
Drain Current-Continuous (Silicon Limited)	I_D	40	A
Drain Current-Continuous($T_C=100^\circ C$)	$I_D (100^\circ C)$	20	A
Pulsed Drain Current (Package Limited)	I_{DM}	160	A

Single pulse avalanche energy	E_{AS}	350	mJ
Maximum power dissipation	P_D	65	W
Operating junction Temperature range	T_j	-55—150	°C

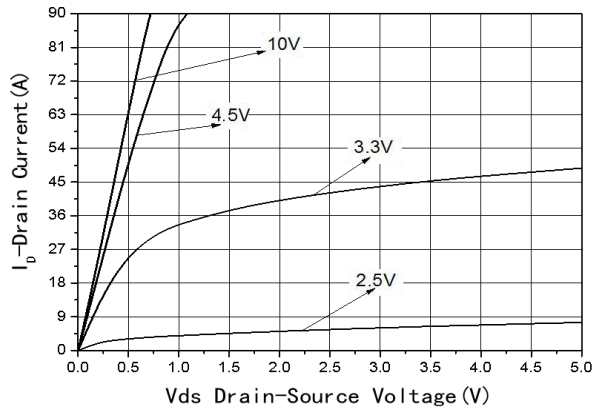
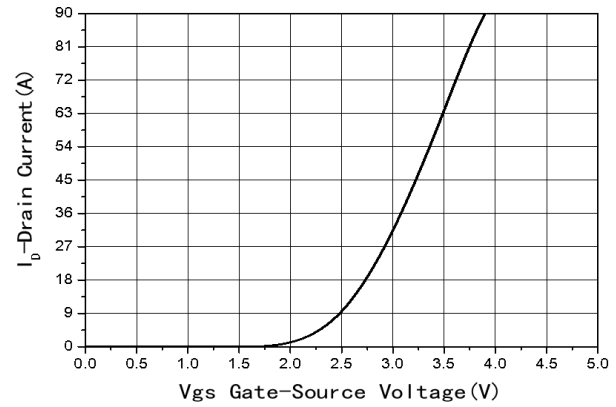
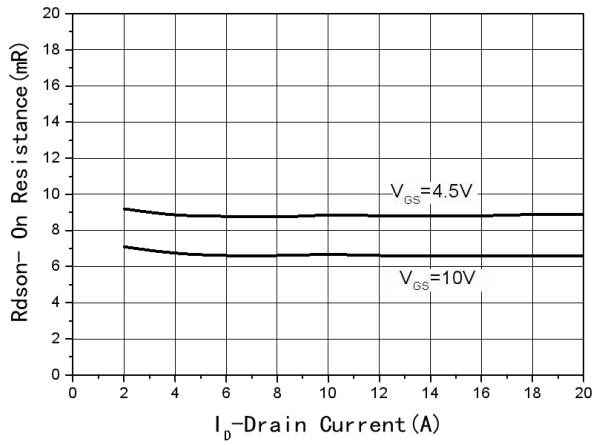
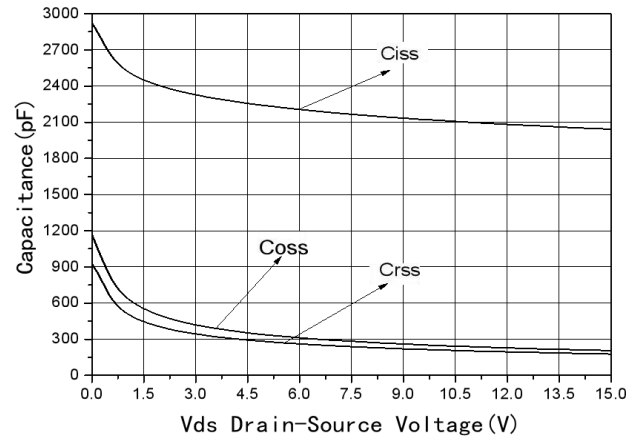
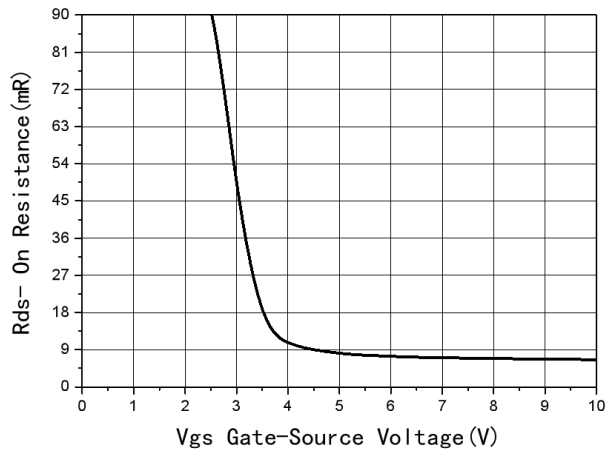
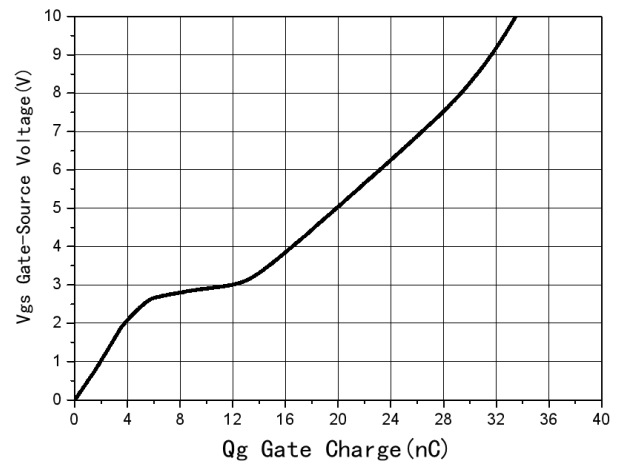
Electrical Characteristics (TA=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
OFF Characteristics						
Drain-source breakdown voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA	40	-	-	V
Zero gate voltage drain current	I _{DSS}	V _{DS} =40V, V _{GS} =0V	-	-	1	μA
Gate-body leakage	I _{GSS}	V _{DS} =0V, V _{GS} =±20V	-	-	±10	μA
ON Characteristics						
Gate threshold voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	1.0	1.5	2	V
Drain-source on-state resistance	R _{DS(ON)}	V _{GS} =10V, I _D =40A	-	6.6	13	mΩ
		V _{GS} =4.5V, I _D =40A	-	9	15	
Forward transconductance	g _{fs}	V _{DS} =5V, I _D =40A	26	30	-	S
Dynamic Characteristics						
Input capacitance	C _{ISS}	V _{DS} =-20V ,V _{GS} =0V f=1.0MHz	-	1991	-	pF
Output capacitance	C _{OSS}		-	180	-	
Reverse transfer capacitance	C _{RSS}		-	156	-	
Switching Characteristics						
Turn-on delay time	t _{D(ON)}	V _{DS} =-20V I _D =-2.8A V _{GEN} =-4.5V R _L =10ohm R _{GEN} =-60ohm	-	14	-	ns
Rise time	t _r		-	18	-	
Turn-off delay time	t _{D(OFF)}		-	50	-	
Fall time	t _f		-	21	-	
Total gate charge	Q _g	V _{DS} =-20V,I _D =-3A V _{GS} =-4.5V	-	33.4	-	nC
Gate-source charge	Q _{gs}		-	5.9	-	
Gate-drain charge	Q _{gd}		-	6.5	-	

Thermal Characteristics

Thermal Resistance junction-to ambient	$R_{th JA}$	100	°C/W
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Typical Performance Characteristics


Fig1 Output Characteristics

Fig2 Transfer Characteristics

Fig3 $R_{DS(on)}$ -Drain current

Fig4 Capacitance vs V_{DS}

Fig5 $R_{DS(on)}$ -Gate Drain voltage

Fig6 Gate Charge

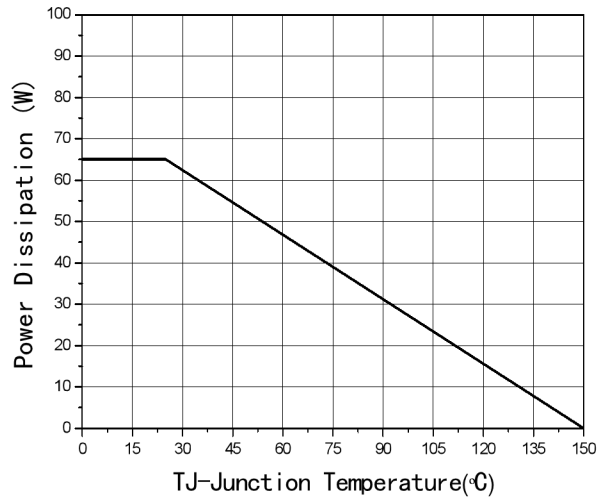


Fig7 Power De-rating

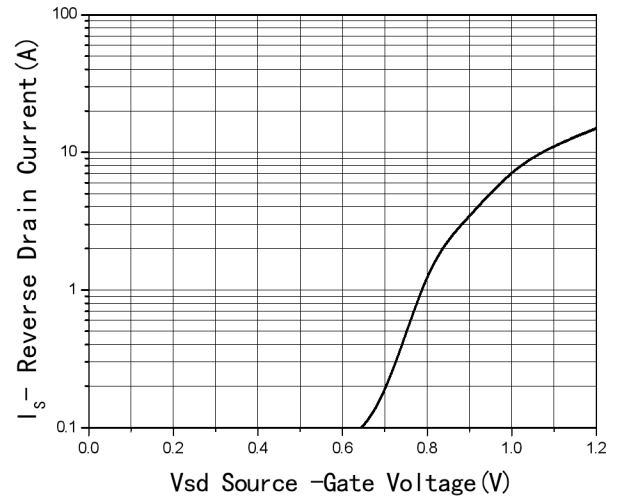
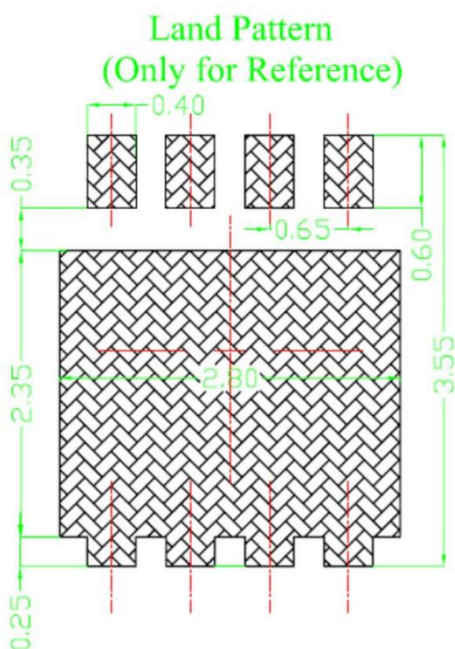
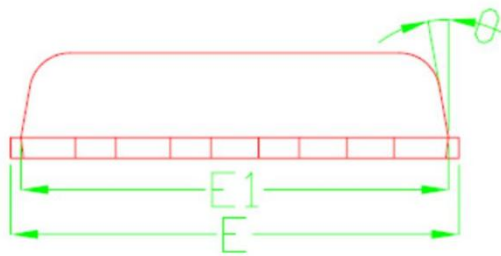
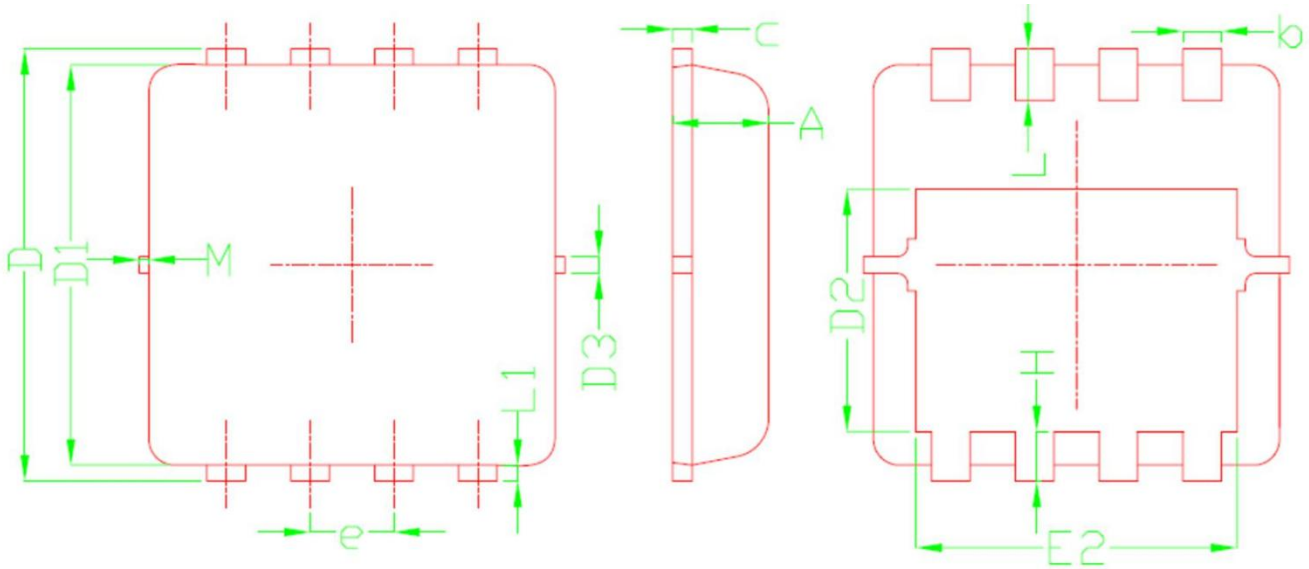


Fig8 Source-Drain Diode Forward

Package Information

- DFN3×3-8L



SYMBOL	DIMENSIONAL REQMTS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
b	0.25	0.30	0.35
c	0.10	0.15	0.25
D	3.25	3.35	3.45
D1	3.00	3.10	3.20
D2	1.78	1.88	1.98
D3	---	0.13	---
E	3.20	3.30	3.40
E1	3.00	3.15	3.20
E2	2.39	2.49	2.59
e	0.65BSC		
H	0.30	0.39	0.50
L	0.30	0.40	0.50
L1	---	0.13	---
θ	---	10°	12°
M	*	*	0.15
* Not specified			