CP55P02QR

20V P-Channel Enhancement Mode MOSFET

Description

The CP55P02QR uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

- V_{DS} =-20V，I_D =-55A
  $R_{DS(ON)}$(Typ.)=5.3mΩ @V_{GS}=-4.5V
  $R_{DS(ON)}$(Typ.)=7.4mΩ @V_{GS}=-2.5V
- High density cell design for ultra low $R_{DS(ON)}$
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation

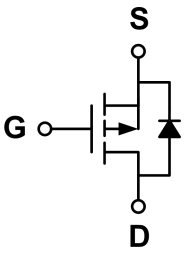
Application

- Load switch

Package

- PDFN3*3-8L

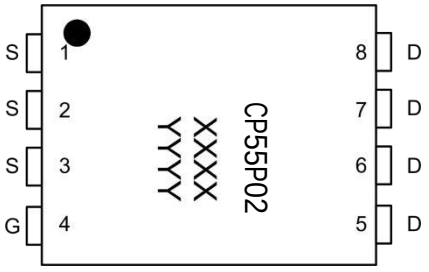
Schematic diagram



Marking and pin assignment

PDFN3×3-8L

（Top View）



Ordering Information

Part Number	Storage Temperature	Package	Devices Per Reel
CP55P02QR-G	-55°C to +150°C	PDFN3*3-8L	5000

Absolute Maximum Ratings (TA=25℃ unless otherwise noted)

parameter		symbol	limit	unit
Drain-source voltage		V_{DS}	-20	V
Gate-source voltage		V_{GS}	±12	V
Continuous Drain Current	TC=25°C	I_D	-55	A
	TC=125°C		-40	
Pulsed Drain Current		I_{DP}	-220	A
Avalanche Current		I_{AS}	-55	A
Avalanche energy(L=1mH) (note1)		E_{AS}	94	mJ
Maximum power dissipation	TC=25°C	P_D	70	W
	TC=100°C		31	
Operating junction Temperature range		Tj	-55—150	℃

Electrical Characteristics (TA=25℃ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static Characteristics						
Drain-source breakdown voltage	BV_{DSS}	V_{GS}=0V, I_D=-250μA	-20	-	-	V
Zero gate voltage drain current	I_{DSS}	V_{DS}=-20V, V_{GS}=0V	-	-	-1	μA
		T_J=85°C	-	-	-30	
Gate Leakage Current	I_{GSS}	V_{DS}=0V, V_{GS}=±12V	-	-	±100	nA
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=-250μA	-0.4	-0.6	-1.0	V
Drain-source on-state resistance[1]	$R_{DS(ON)}$	V_{GS}=-4.5V, I_D=-10A	-	5.3	7	mΩ
		V_{GS}=-2.5V, I_D=-10A	-	7.4	9	
Forward Transconductance	g_{FS}	V_{DS}=-10V, I_D=-10A	-	90	-	S
Diode Characteristics						
Diode Forward Voltage[1]	V_{SD}	I_{SD}=-10A,V_{GS}=0V	-	-0.72	-1.5	V
Diode Continuous Forward Current	I_S		-	-	-50	A
Reverse Recovery Time	t_{rr}	I_F=-10A, dI/dt=-100A/us	-	30	-	ns
Reverse Recovery Charge	Q_{rr}		-	75	-	nC
Dynamic Characteristics[2]						
Gate Resistance	R_G	V_{GS}=0V,V_{DS}=0V, f=1MHz	-	13	-	Ω
Input capacitance	C_{ISS}	V_{GS}=0V ,V_{DS}=-10V f=1.0MHz	-	3626	-	pF
Output capacitance	C_{OSS}		-	547	-	
Reverse transfer capacitance	C_{RSS}		-	479	-	
Turn-on delay time	$t_{D(ON)}$	V_{GS}=-10V, V_{DS}=-10V, R_L=1.5Ω, R_G=3Ω	-	7	-	ns
Turn-on Rise time	tr		-	12	-	
Turn-off delay time	$t_{D(OFF)}$		-	134	-	
Turn-off Fall time	tf		-	45	-	
Total gate charge	Q_g	V_{GS}=-5V,I_D=-10A V_{DS}=-10V	-	45		nC
Gate-source charge	Q_{gs}			36		
Gate-drain charge	Q_{gd}		-	8	-	

Note: 1：Pulse test; pulse width ≦ 300ns, duty cycle ≦ 2%.

2：Guaranteed by design, not subject to production testing.

Thermal Characteristics

Parameter	Symbol	Typical	Unit
Thermal Resistance-Junction to Case	$R_{\theta JC}$	1.7	℃/W
Thermal Resistance junction-to ambient	$R_{\theta JA}$	62.5	

Typical Performance Characteristics

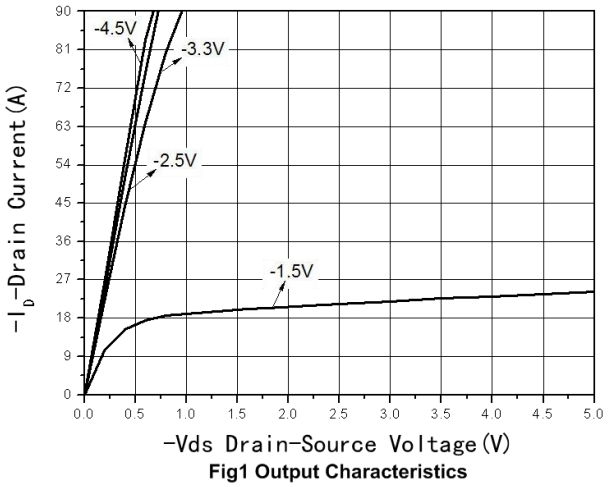


Fig1 Output Characteristics

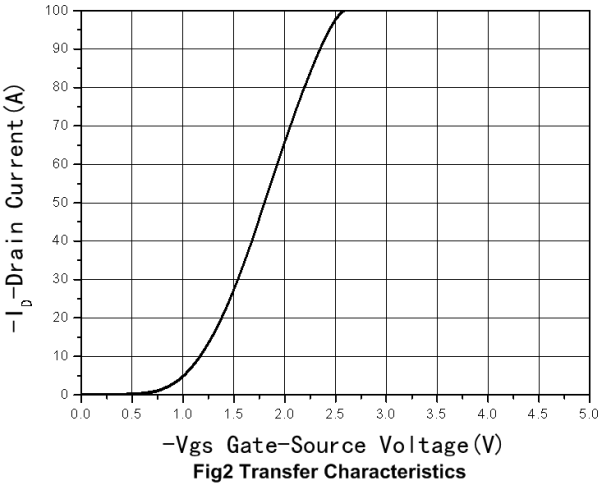


Fig2 Transfer Characteristics

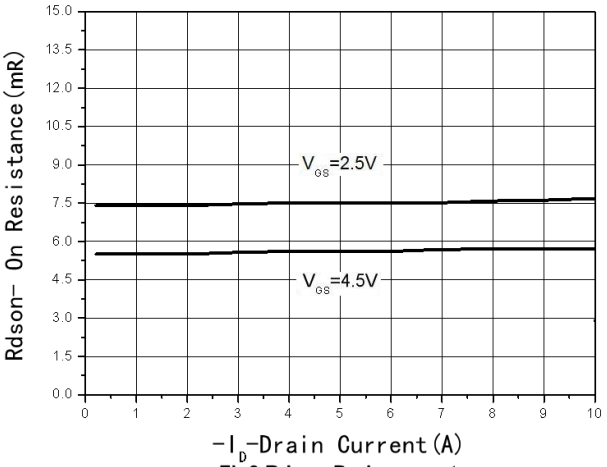


Fig3 Rdson-Drain current

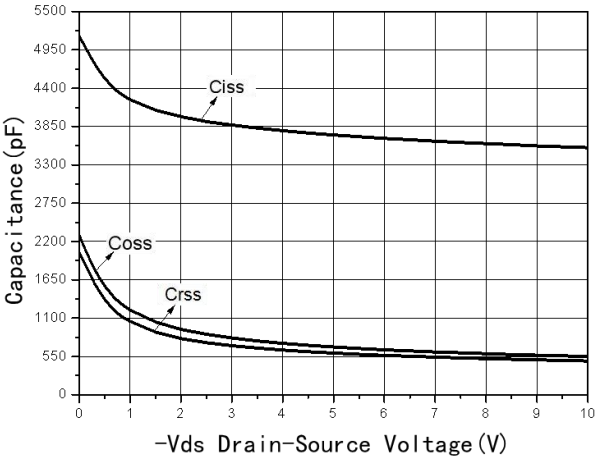


Fig4 Capacitance vs Vds

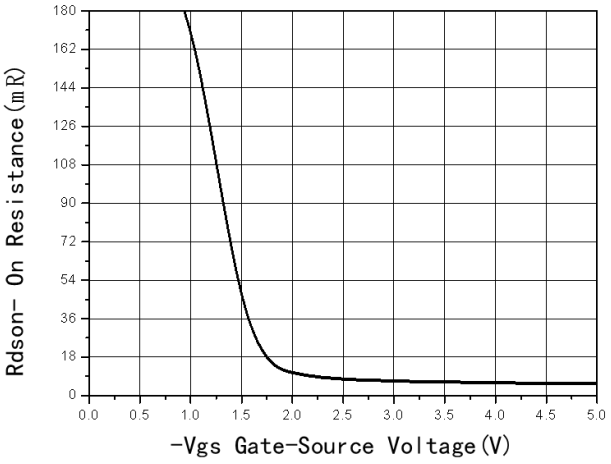


Fig5 Rdson-Gate Drain voltage

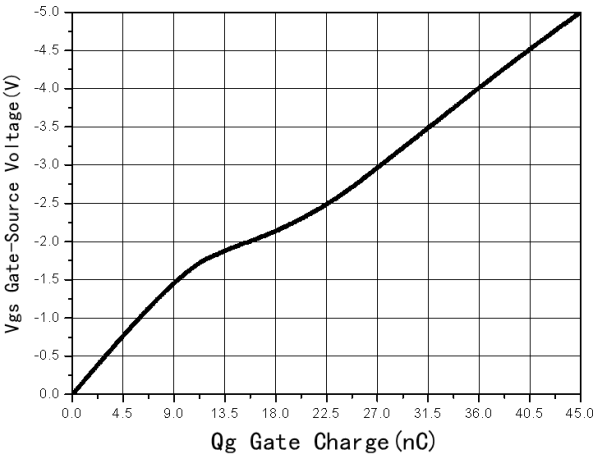


Fig6 Gate Charge

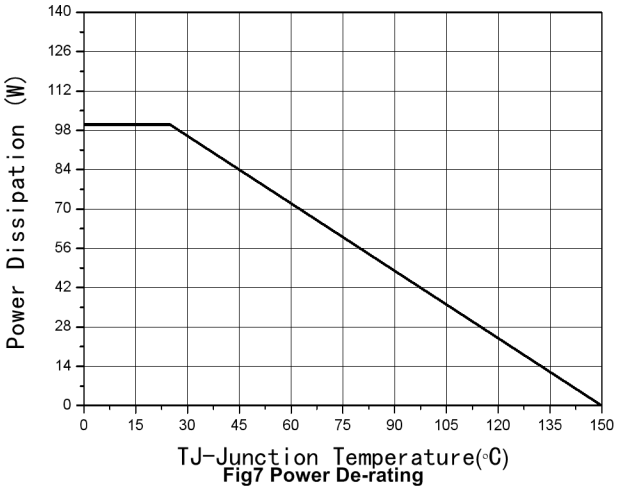


Fig7 Power De-rating

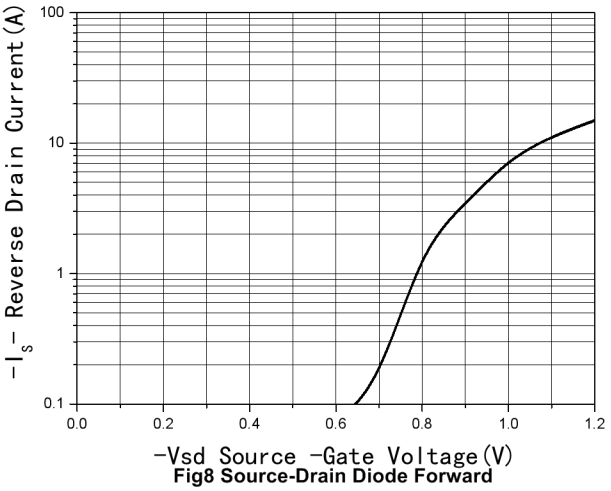
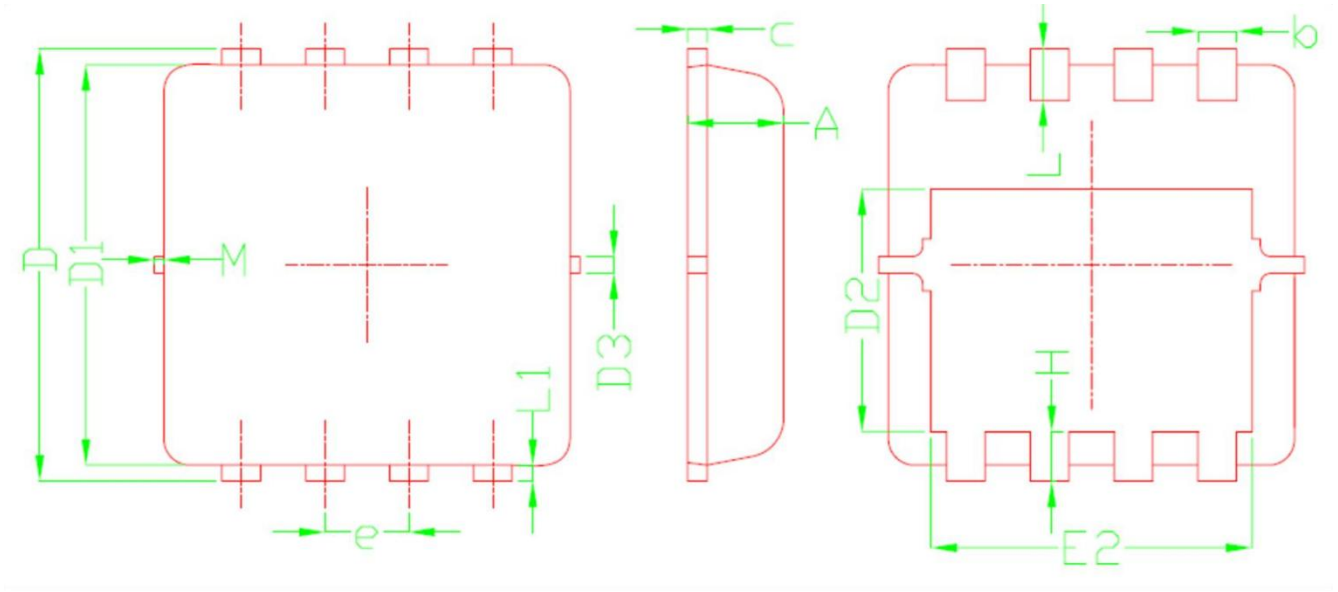
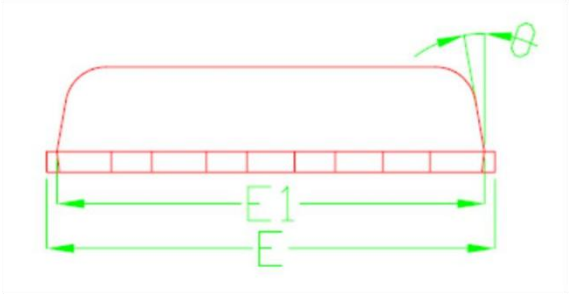


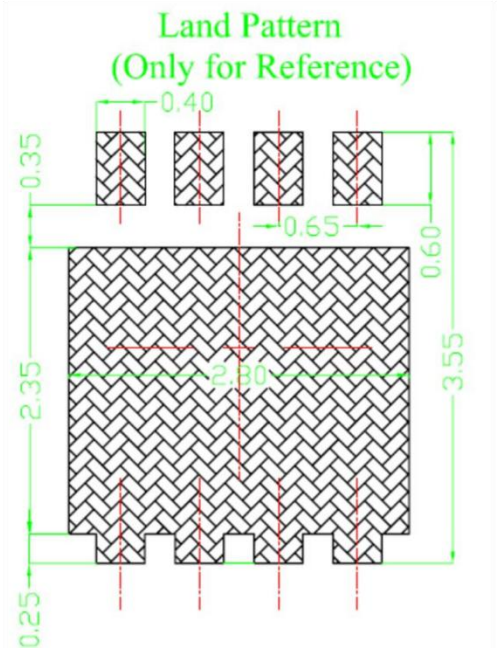
Fig8 Source-Drain Diode Forward

Package Information

- **PDFN3*3-8L**







SYMBOL	DIMENSIONAL REQMTS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
b	0.25	0.30	0.35
c	0.10	0.15	0.25
D	3.25	3.35	3.45
D1	3.00	3.10	3.20
D2	1.78	1.88	1.98
D3	---	0.13	---
E	3.20	3.30	3.40
E1	3.00	3.15	3.20
E2	2.39	2.49	2.59
e	0.65BSC		
H	0.30	0.39	0.50
L	0.30	0.40	0.50
L1	---	0.13	---
θ	---	10°	12°
M	*	*	0.15
* Not specified			