★ 100% EAS Guaranteed
★ Green Device Available
★ Super Low Gate Charge
★ Excellent CdV/dt effect decline
★ Advanced high cell density Trench technology

Product Summary

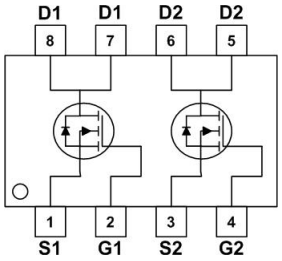
BVDSS	RDSON	ID
30V	12mΩ	30A

Description

The CP302 is the high cell density trenched N-ch MOSFETs, which provide excellent RDSON and gate charge for most of the synchronous buck converter applications.

The CP302 meet the RoHS and Green Product requirement 100% EAS guaranteed with full function reliability approved.

DFN3X3-8 Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	30	V
V_{GS}	Gate-Source Voltage	±20	V
I_D@T_A=25°C	Continuous Drain Current, V_{GS} @ 10V[1]	30	A
I_D@T_A=70°C	Continuous Drain Current, V_{GS} @ 10V[1]	18	A
I_{DM}	Pulsed Drain Current[2]	50	A
EAS	Single Pulse Avalanche Energy[3]	24.2	mJ
I_{AS}	Avalanche Current	22	A
P_D@T_A=25°C	Total Power Dissipation[4]	1.5	W
T_{STG}	Storage Temperature Range	-55 to 150	°C
T_J	Operating Junction Temperature Range	-55 to 150	°C

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient [1]	---	85	°C/W
$R_{\theta JL}$	Thermal Resistance Junction-Case[1]	---	25	°C/W

Electrical Characteristics (T_J=25 ℃, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V , I_D=250uA	30	---	---	V
$\triangle BV_{DSS}/\triangle T_J$	BVDSS Temperature Coefficient	Reference to 25℃ , I_D=1mA	---	0.023	---	V/℃
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=10V , I_D=8A	---	10	12	mΩ
		V_{GS}=4.5V , I_D=6A	---	15	18	
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS}=V_{DS} , I_D =250uA	1.2	---	2.5	V
$\triangle V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	-5.08	---	mV/℃
I_{DSS}	Drain-Source Leakage Current	V_{DS}=24V , V_{GS}=0V , T_J=25℃	---	---	1	uA
		V_{DS}=24V , V_{GS}=0V , T_J=55℃	---	---	5	
I_{GSS}	Gate-Source Leakage Current	V_{GS} =±20V , V_{DS}=0V	---	---	±100	nA
gfs	Forward Transconductance	V_{DS}=5V , I_D=8A	---	24	---	S
R_g	Gate Resistance	V_{DS}=0V , V_{GS}=0V , f=1MHz	---	1.8	---	Ω
Q_g	Total Gate Charge (4.5V)	V_{DS}=15V , V_{GS}=4.5V , I_D=8A	---	9.63	---	nC
Q_{gs}	Gate-Source Charge		---	3.88	---	
Q_{gd}	Gate-Drain Charge		---	3.44	---	
$T_{d(on)}$	Turn-On Delay Time	V_{DD}=15V , V_{GS}=10V , R_G=1.5Ω I_D=8A	---	4.2	---	ns
T_r	Rise Time		---	8.2	---	
$T_{d(off)}$	Turn-Off Delay Time		---	31	---	
T_f	Fall Time		---	4	---	
C_{iss}	Input Capacitance	V_{DS}=15V , V_{GS}=0V , f=1MHz	---	940	---	pF
C_{oss}	Output Capacitance		---	131	---	
C_{rss}	Reverse Transfer Capacitance		---	109	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current[1,5]	V_G=V_D=0V , Force Current	---	---	9	A
V_{SD}	Diode Forward Voltage[2]	V_{GS}=0V , I_S=1A , T_J=25℃	---	---	1	V
t_{rr}	Reverse Recovery Time	I_F=8A , di/dt=100A/μs , T_J=25℃	---	8	---	nS
Q_{rr}	Reverse Recovery Charge		---	2.9	---	nC

Note :
1. The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper.
2. The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%
3. The EAS data shows Max. rating . The test condition is V_{DD}=25V,V_{GS}=10V,L=0.1mH,I_{AS}=22A
4. The power dissipation is limited by 150℃ junction temperature
5. The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Characteristics

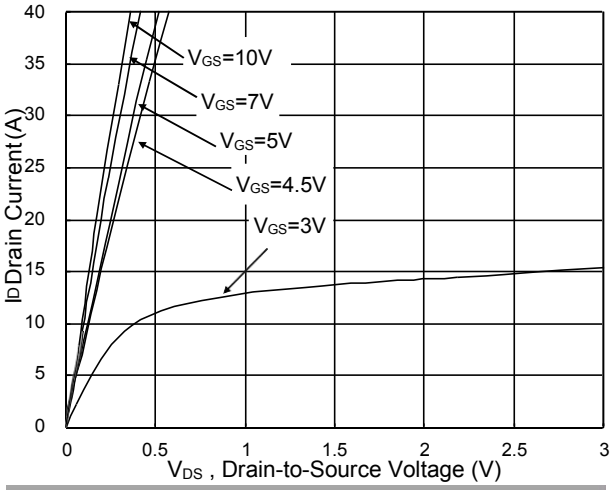


Fig.1 Typical Output Characteristics

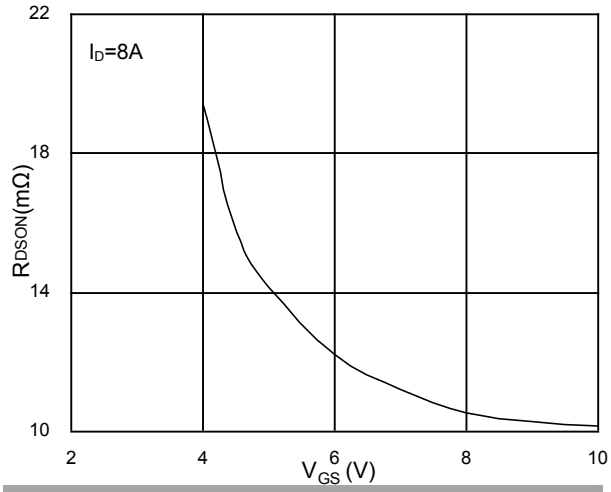


Fig.2 On-Resistance vs. G-S Voltage

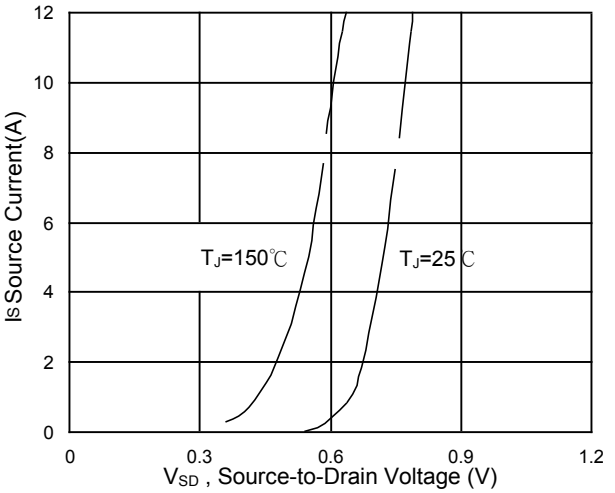


Fig.3 Source Drain Forward Characteristics

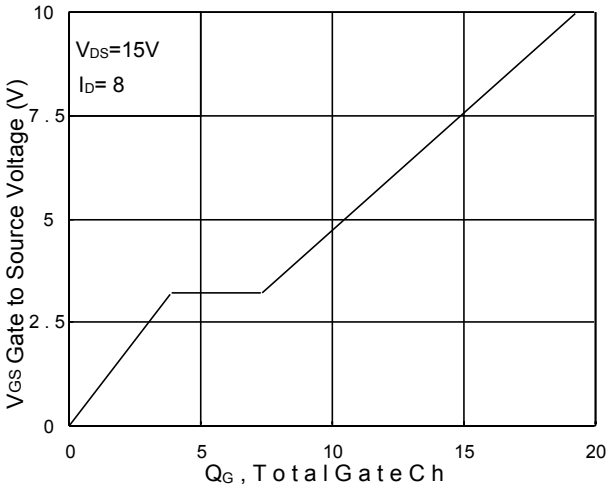


Fig.4 Gate-Charge Characteristics

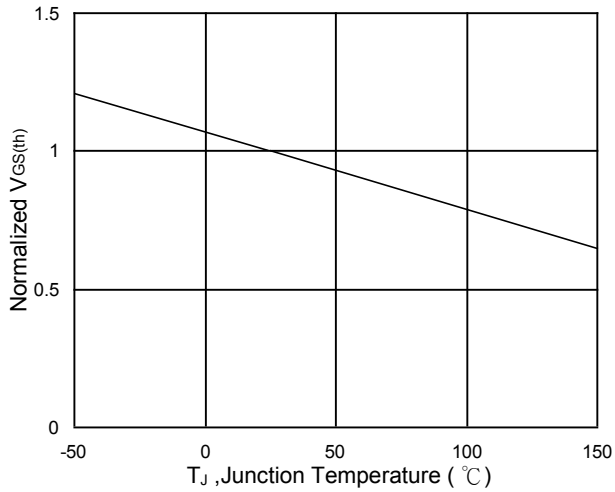


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

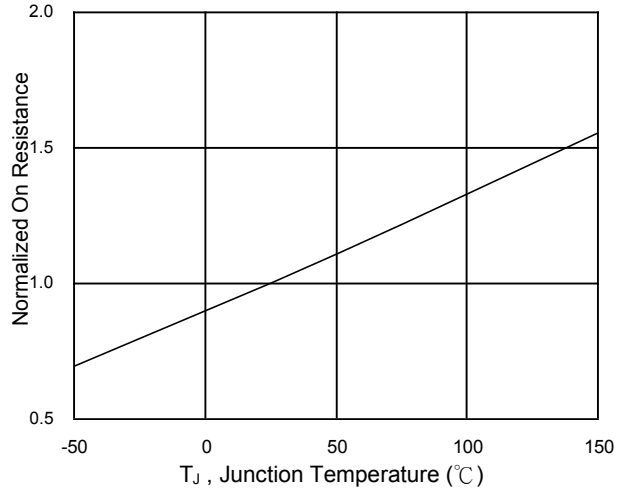


Fig.6 Normalized R_{DSON} vs. T_J

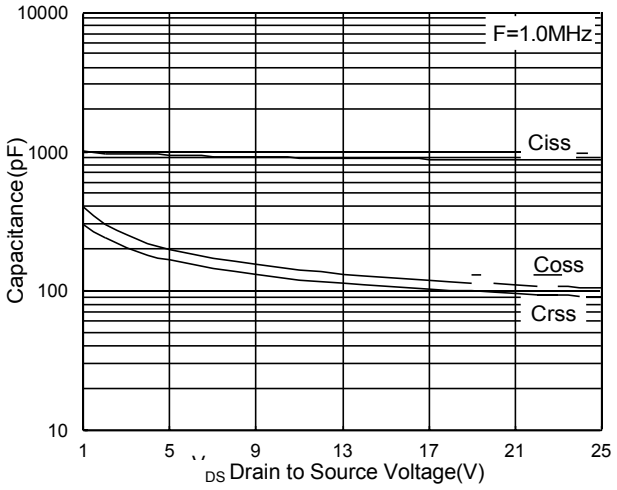


Fig.7 Capacitance

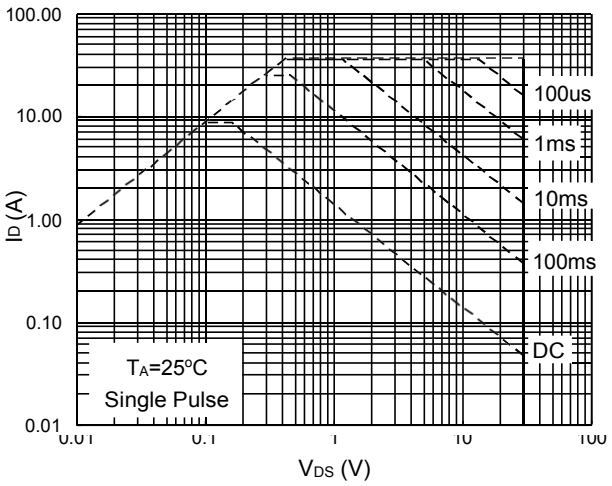


Fig.8 Safe Operating Area

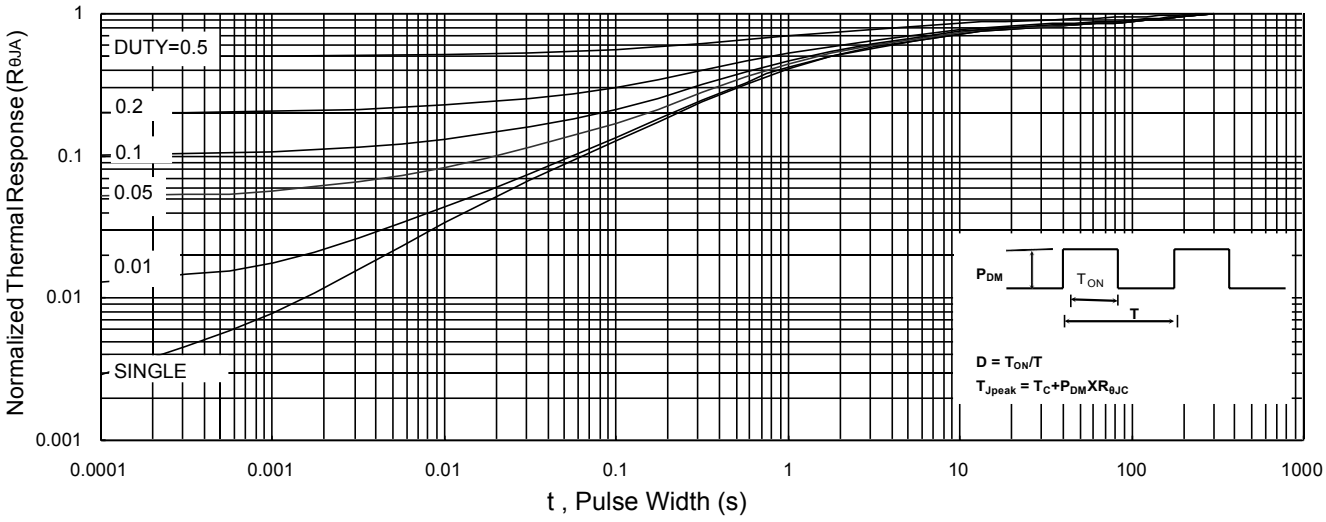
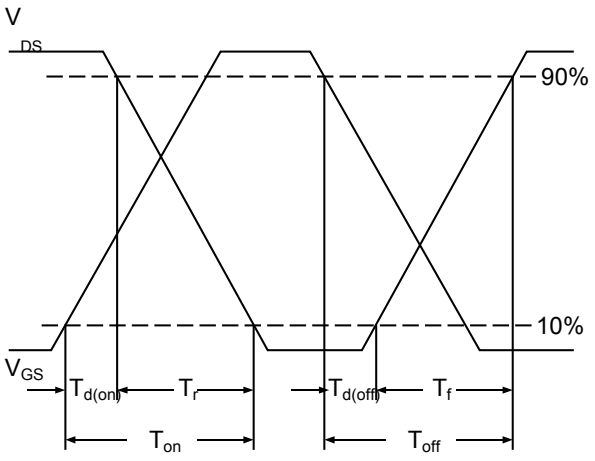
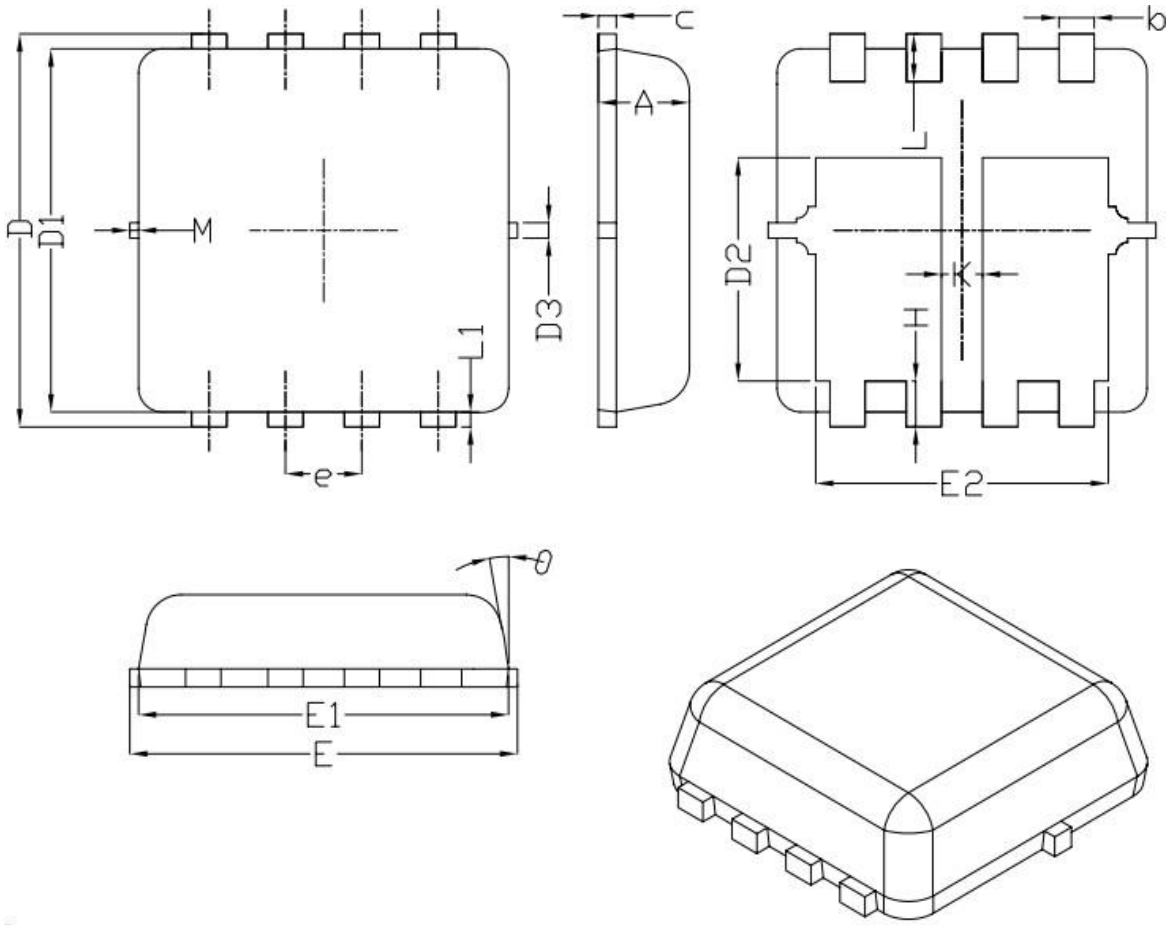


Fig.9 Normalized Maximum Transient Thermal Impedance



$$EAS=\frac{1}{2} L \times I_{AS}^2 \times \frac{BV_{DSS}}{}$$

Dual DFN3X3 Package Outline Data



Symbol	Dimensions (unit: mm)		
	Min	Typ	Max
A	0.70	0.75	0.80
b	0.25	0.30	0.35
c	0.10	0.15	0.25
D	3.25	3.35	3.45
D1	3.00	3.10	3.20
D2	1.78	1.88	1.98
D3	--	0.13	--
E	3.20	3.30	3.40
E1	3.00	3.15	3.20
E2	2.39	2.49	2.59
e	0.65 BSC		
H	0.30	0.39	0.50
L	0.30	0.40	0.50
L1	--	0.13	--
K	0.30	--	--
θ	--	10°	12°
M	*	*	0.15
* Not Specified			

Notes:

1. Refer to JEDEC MO-240 variation CA.
2. Dimensions "D1" and "E1" do NOT include mold flash protrusions or gate burrs.
3. Dimensions "D1" and "E1" include interterminal flash or protrusion.