Asymmetric LDO Enhancement-Mode MOSFET

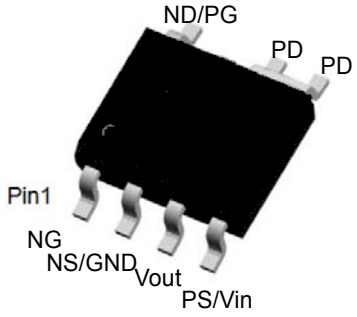
General Description

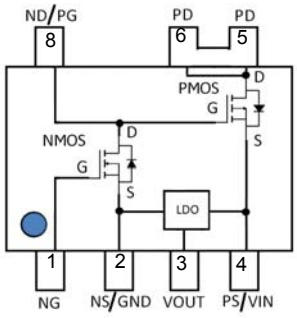
- Low gate charge.
- Use as a load switch.
- Use in PWM applications

Product Summary

N-Channel	P-Channel
• BV_{DSS} = 25V	• BV_{DSS} = -25V
• $R_{DS(on)}$ (@VGS= 10V) 25mΩ(Typ.)	• $R_{DS(on)}$ (@VGS= -10V) 50mΩ(Typ.)
• $R_{DS(on)}$ (@VGS= 4.5V) 28mΩ(Typ.)	• $R_{DS(on)}$ (@VGS= -4.5V) 60mΩ(Typ.)

SOP-7





Absolute Maximum Ratings (T_A = 25°C unless otherwise noted)

MOSFET

Parameter	Symbol	Maximum		Units
		N-Channel	P-Channel	
Drain-Source Voltage	V_{DS}	25	-25	V
Gate-Source Voltage	V_{GS}	±12	±12	V
Drain Current (T_A=25ºC,t<10s,Vgs=10V)	I_D	3.0	-2.8	A
Drain Current (T_A=75ºC,t<10s, Vgs=10V)		1.8	-1.8	A
Pulsed Drain Current [a]	I_{DM}	12	-8	A
Power Dissipation [b] (T_A=25ºC)	P_D	1.25	1.25	W
Power Dissipation [b] (T_A=75ºC)		1.0	0.9	W
Junction and Storage Temperature Range	T_J, T_{STG}	-55 ~ +150	-55 ~ +150	ºC
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Voltage in	Vin	20		V
Power Dissipatin (T_A=25ºC)	P_D	200~450		mW
Junction and Storage Temperature Range	T_J, T_{STG}	-55 ~ +150		ºC

N-Channel Electrical Characteristics (T_A = 25°C unless otherwise noted)						
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Units**
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0V , I_D = 250uA	25			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 25V , V_{GS} = 0V			1	uA
I_{GSS}	Gate-Body Leakage Current	V_{GS} = ±12V, V_{DS} = 0V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS} , I_D = 250uA	0.6		1.2	V
$R_{DS(ON))}$	Drain-Source On-State Resistance	V_{GS} = 10V , I_D = 4.0A		25	35	mΩ
		V_{GS} = 4.5V , I_D = 3.5A		28	45	mΩ
g_{FS}	Forward Transconductance	V_{DS} = 5V , I_D = 4.5A		20		S
V_{SD}	Diode Forward Voltage	V_{GS} = 0V , I_S = 1.0A			1.2	V
I_S	Maximum Body-Diode Continuous Current				2.0	A
C_{iss}	Input Capacitance	V_{DS} = 15V , V_{GS} = 0V f = 1.0MHz		760		pF
C_{oss}	Output Capacitance			83		pF
C_{rss}	Reverse Transfer Capacitance			64		pF
Q_g	Total Gate Charge	V_{DS} = 15V , I_D = 5.8A V_{GS} = 6V		8.5		nC
Q_{gs}	Gate-Source Charge			2.1		nC
Q_{gd}	Gate-Drain Charge			2.6		nC
$t_{D(ON)}$	Turn-On Delay Time	V_{DD} = 15V , ID = 1A V_{GS} = 6 V R_{GEN} = 6 ohm		4		ns
t_r	Turn-On Rise Time			3.2		ns
$t_{D(OFF)}$	Turn-Off Delay Time			28		ns
t_f	Turn-Off Fall Time			6		ns

P-Channel Electrical Characteristics (T_A = 25°C unless otherwise noted)						
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Units**
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0V , I_D = -250uA	-25			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -25V , V_{GS} = 0V			-1	uA
I_{GSS}	Gate-Body Leakage Current	V_{GS} = ±12V, V_{DS} = 0V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS} , I_D = -250uA	-0.5		-1.2	V
$R_{DS(ON))}$	Drain-Source On-State Resistance	V_{GS} = -10V , I_D = -3.0A		50	65	mΩ
		V_{GS} = -4.5V , I_D = -2.5A		60	75	mΩ
g_{FS}	Forward Transconductance	V_{DS} = -10V , I_D = -4.0A		15		S
V_{SD}	Diode Forward Voltage	V_{GS} = 0V , I_S = -1.0A			-1.2	V
I_S	Maximum Body-Diode Continuous Current				-2.0	A
C_{iss}	Input Capacitance	V_{DS} = -15V , V_{GS} = 0V f = 1.0MHz		1020		pF
C_{oss}	Output Capacitance			125		pF
C_{rss}	Reverse Transfer Capacitance			85		pF
Q_g	Total Gate Charge	V_{DS} = -15V , I_D = -5.2A V_{GS} = -6V		10.5		nC
Q_{gs}	Gate-Source Charge			3.5		nC
Q_{gd}	Gate-Drain Charge			4.0		nC
$t_{D(ON)}$	Turn-On Delay Time	V_{DD} = -15V , ID = -1A V_{GS} = -6 V R_{GEN} = 6 ohm		7.5		ns
t_r	Turn-On Rise Time			4.5		ns
$t_{D(OFF)}$	Turn-Off Delay Time			45.5		ns
t_f	Turn-Off Fall Time			15		ns

a. Repetitive rating, Pulse width limited by junction temperature $T_{J(MAX)}$=150 ºC. Ratings are based on low frequency and duty cycles to keep initial T_J=25 ºC

b. The power dissipation P_D is based on $T_{J(MAX)}$=150 ºC , using≤10s junction-to-ambient thermal resistance.

c. The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A = 25°C. The value in any given application depends on the user's specific board design.

d. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to lead $R_{\theta JL}$ and lead to ambient.

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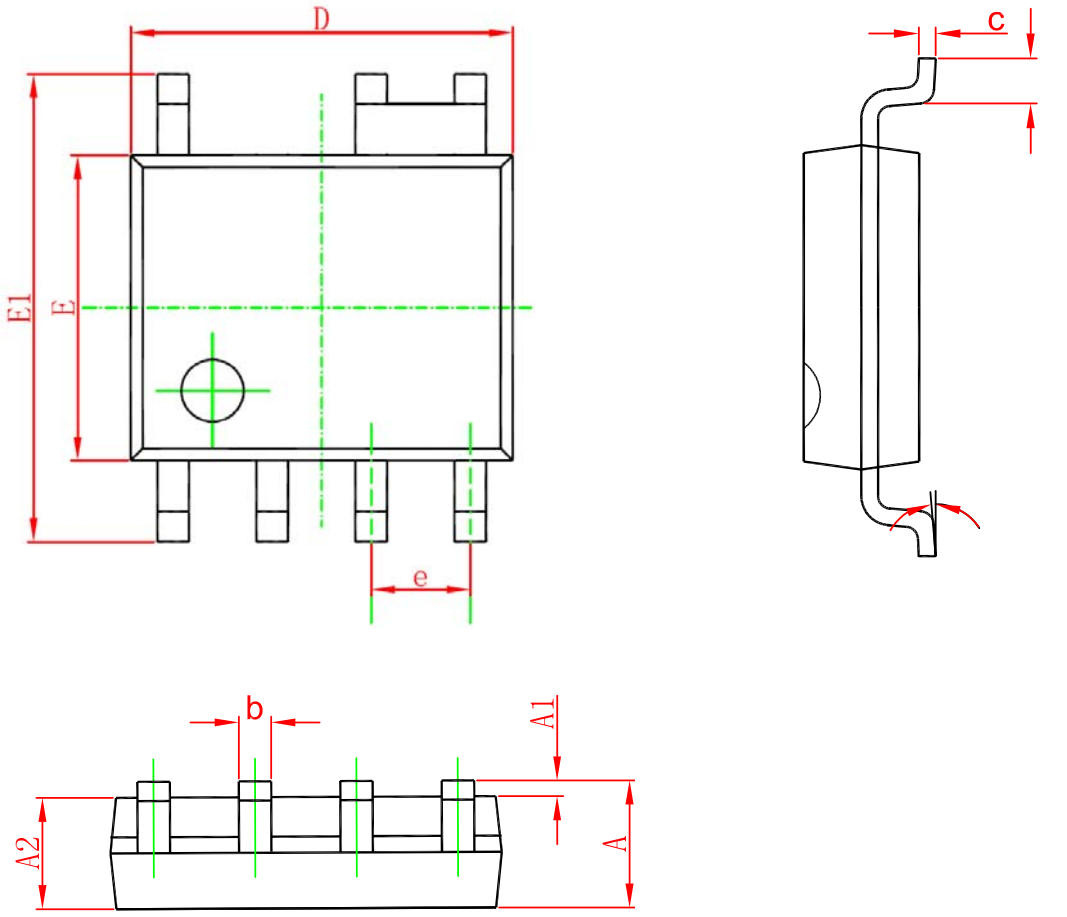
参　数	测试条件	最小值	典型值	最大值	单位
V_{OUT}　输出电压	VCC1=7V,I_{OUT}=1mA	4.85	5	5.15	V
I_{OUT}　输出电流	VCC1=7V	60	100	-	mA
ΔV_{OUT}　负载调节	VCC1=7V，1mA≤I_{OUT}≤30mA	-	60	150	mV
V_{DIF}　跌落电压	I_{OUT}=1mA	-	100	-	mV
I_{SS}　静态电流	VCC1=7V，空载	-	2	3	uA
$\Delta V_{OUT}/\Delta VCC1/V_{OUT}$ 线性调整	6V≤VCC1≤18V，I_{OUT}=1mA	-	0.2	-	%/V
V_{IN}　输入电压	-	-	-	18	V
$\Delta V_{OUT}/\Delta T_A/V_{OUT}$ 温度系数	VCC1=7V，I_{OUT}=10mA 0℃≤T_A≤70℃	-	100	-	ppm/℃

SOP-7 Package Outline



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°