# 5.5V 1A 1.5MHz Synchronous Step-Down Regulator

## Features

- High Efficiency: Up to 96%
- 2.5V to 5.5V Input Voltage Range
- 1.5MHz Constant Frequency Operation
- No Schottky Diode Required
- Low Dropout Operation: 100% Duty Cycle
- PFM Mode for High Efficiency in Light Load
- Over Temperature Protected
- Low Quiescent Current: 40μA
- Short Circuit Protection
- Inrush Current Limit and Soft Start
- 1A Continuous Output Current
- SOT23-5 package

## Applications

- Cellular and Smart Phones
- Wireless and DSL Modems
- PDAs
- Portable Instruments
- Digital Still and Video Cameras
- PC Cards

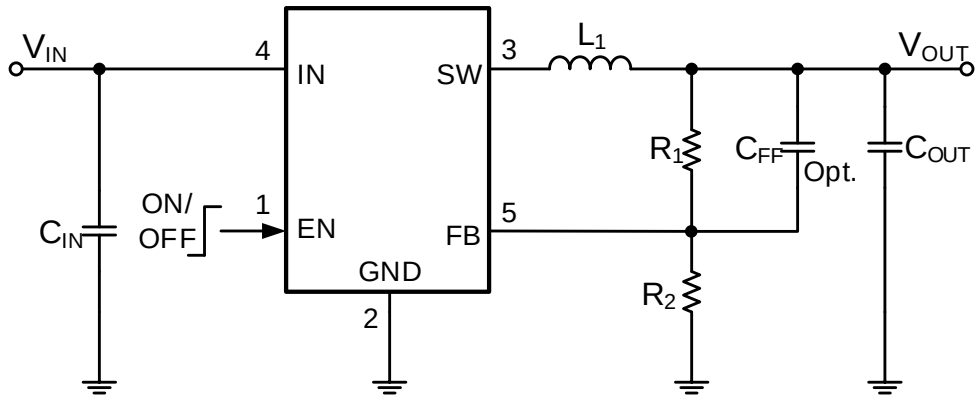
## General Description

The PT62568 is a high-efficiency monolithic synchronous buck regulator using a constant frequency, current mode architecture. The device is available in an adjustable version. Supply current with no load is 40uA and drops to <1uA in shutdown. The 2.5V to 5.5V input voltage range makes the PT62568 ideally suited for single Li-Ion battery powered applications. 100% duty cycle provides low dropout operation, extending battery life in portable systems. PWM/PFM mode operation provides very low output ripple voltage for noise sensitive applications.

Switching frequency is internally set at 1.5MHz, allowing the use of small surface mount inductors and capacitors. Low output voltages are easily supported with the 0.6V feedback reference voltage.

The PT62568is offered in a low profile (1mm) 5-pin, thin SOT package, and is available in an adjustable version

## . Typical Application Circuit




Basic Application Circuit

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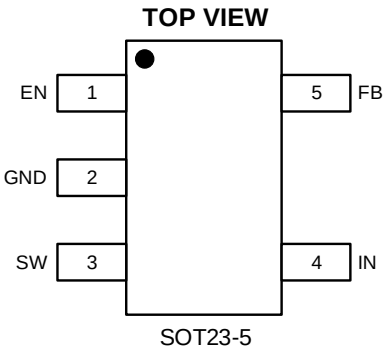
## Pin Description

### Pin Configuration




### Pin Description

| Pin | Name | Function |
|---|---|---|
| 1 | EN | Chip Enable Pin. Drive EN above 1.5V to turn on the part. Drive EN below 0.3V to turn it off. Do not leave EN floating. |
| 2 | GND | Ground Pin |
| 3 | SW | Power Switch Output. It is the switch node connection to Inductor. This pin connects to the drains of the internal P-ch and N-ch MOSFET switches. |
| 4 | IN | Power Supply Input. Must be closely decoupled to GND with a 10μF or greater ceramic capacitor. |
| 5 | FB | Output Voltage Feedback Pin. An internal resistive divider divides the output voltage down for comparison to the internal reference voltage. |

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## Absolute Maximum Ratings (1)(2)

Input Supply Voltage …… -0.3V to 6.0V
EN, FB Voltages……..... -0.3V to 6.0V
SW Voltage…….…. -0.3V to (Vin+0.3V)
Peak SW Sink and Source Current ……3A
Thermal Resistance ( θJA) …… 170 °C/W
ESD(Human Body Made)HMB……2KV

Operating Temperature Range ……..... -40°C to +85°C
Junction Temperature(Note2) ……...…... 150°C
Storage Temperature Range ...…...…...…. -65°C to 150°C
Lead Temperature(Soldering,10s)……. +300°C
Thermal Resistance（θJC） SOT23-5…… 130 °C/W
ESD (Machine Made)MM……200V

Note (1): Exceeding these ratings may damage the device.
Note (2): The device is not guaranteed to function outside of its operating conditions.

## Electrical Characteristics (1)(2)

($V_{IN}$=$V_{EN}$=3.6V, $T_A$ = 25°C, unless otherwise noted.)

| Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Input Voltage Range | | 2.5 | | 5.5 | V |
| UVLO Threshold | | | 2.4 | | V |
| Input DC Supply Current | FB = 90%, Iload=0mA | | 150 | 300 | μA |
| | FB= 105%, Iload=0mA | | 40 | 70 | μA |
| | $V_{EN}$ = 0V, $V_{IN}$=4.2V | | 0.1 | 1.0 | μA |
| Regulated Feedback Voltage | $T_A$ = 25°C | 0.588 | 0.600 | 0.612 | V |
| Reference Voltage Line Regulation | Vin = 2.5V to 5.5V | | 0.04 | 0.40 | %/V |
| Output Voltage Line Regulation | $V_{IN}$ = 2.5V to 5.5V | | 0.04 | 0.4 | % |
| Output Voltage Load Regulation | | | 0.5 | | % |
| Oscillation Frequency | | | 1.5 | | MHz |
| On Resistance of PMOS | $I_{SW}$=100mA | | 0.3 | | Ω |
| ON Resistance of NMOS | $I_{SW}$=-100mA | | 0.2 | | Ω |
| Peak Current Limit | $V_{IN}$= 3.6V, FB=90% | 1.5 | | | A |
| EN Threshold | | | 1.0 | | V |
| EN Leakage Current | | | ±0.01 | ±1.0 | μA |
| SW Leakage Current | $V_{EN}$=0V,$V_{IN}$=Vsw=5V | | ±0.01 | ±1.0 | μA |
| Soft Start | | | | 1.2 | mS |
| Thermal Shutdown | | | 160 | | ℃ |
| Thermal Hysteresis | | | 20 | | ℃ |

Note (1): MOSFET on-resistance specifications are guaranteed by correlation to wafer level measurements.
Note (2): Thermal shutdown specifications are guaranteed by correlation to the design and characteristics analysis.

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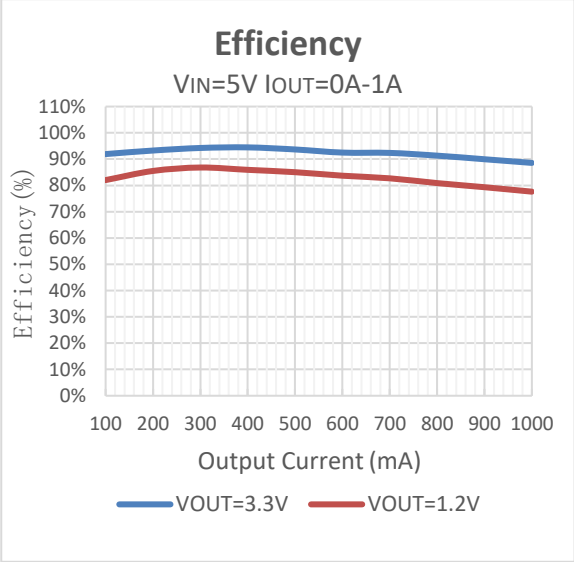
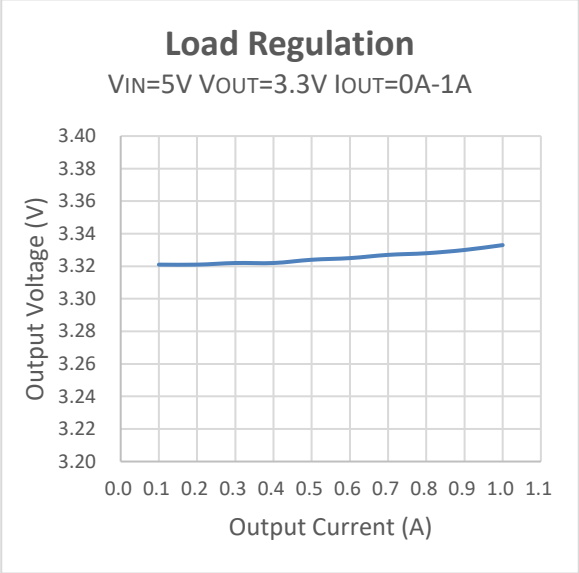
## Typical Performance Characteristics

### Efficiency

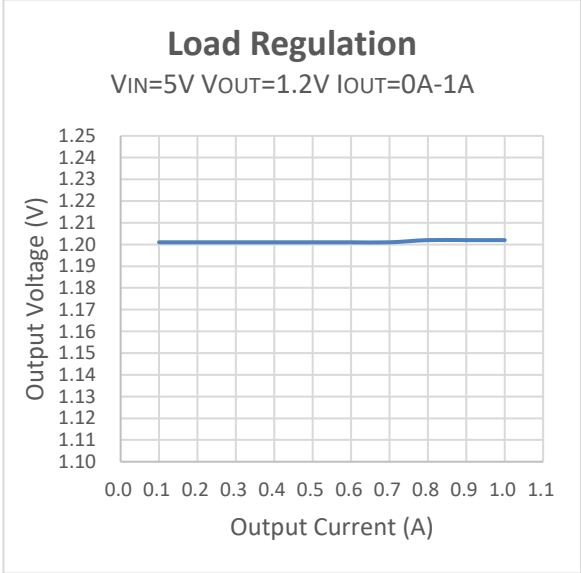



Efficiency $V_{OUT}$=3.3V vs 1.2V

### Load Regulation




Load Regulation $V_{OUT}$=3.3V




Load Regulation $V_{OUT}$=1.2V

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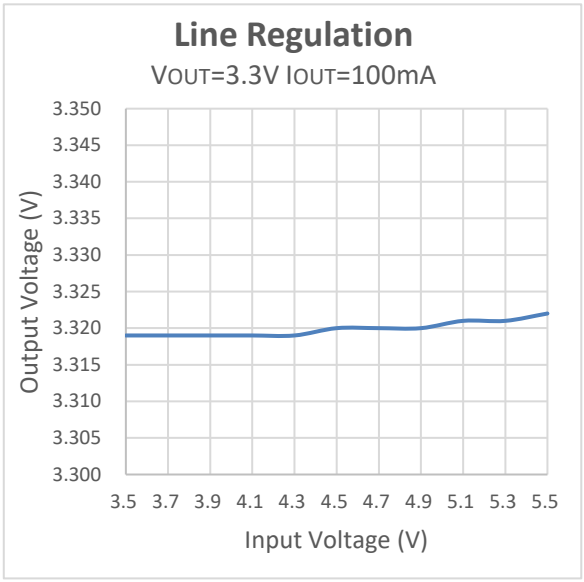
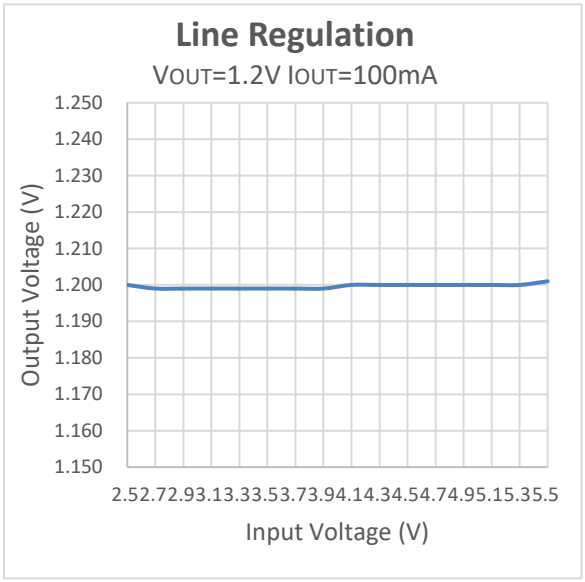
## Line Regulation

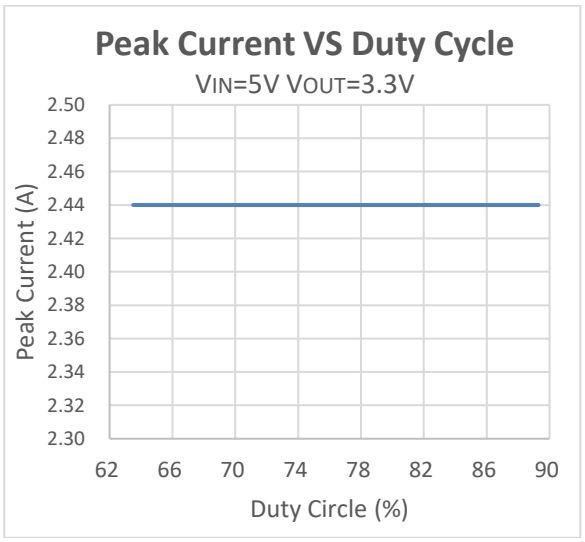



Line Regulation $V_{OUT}$=3.3V




Line Regulation $V_{OUT}$=1.2V

## Peak Current VS Duty Circle




Peak Current VS Duty Circle

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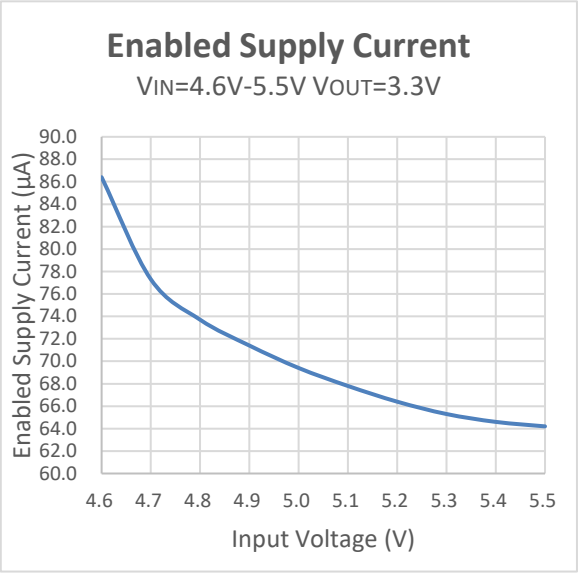
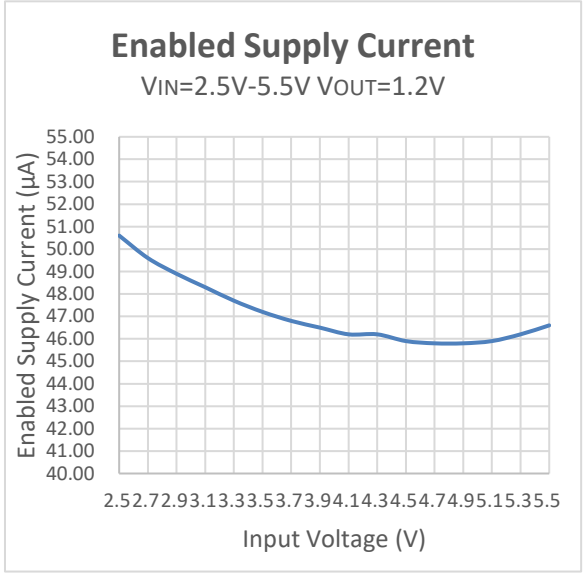
## Enabled Supply Current VS Input Voltage




Enabled Supply Current $V_{OUT}$=3.3V




Enabled Supply Current $V_{OUT}$=1.2V

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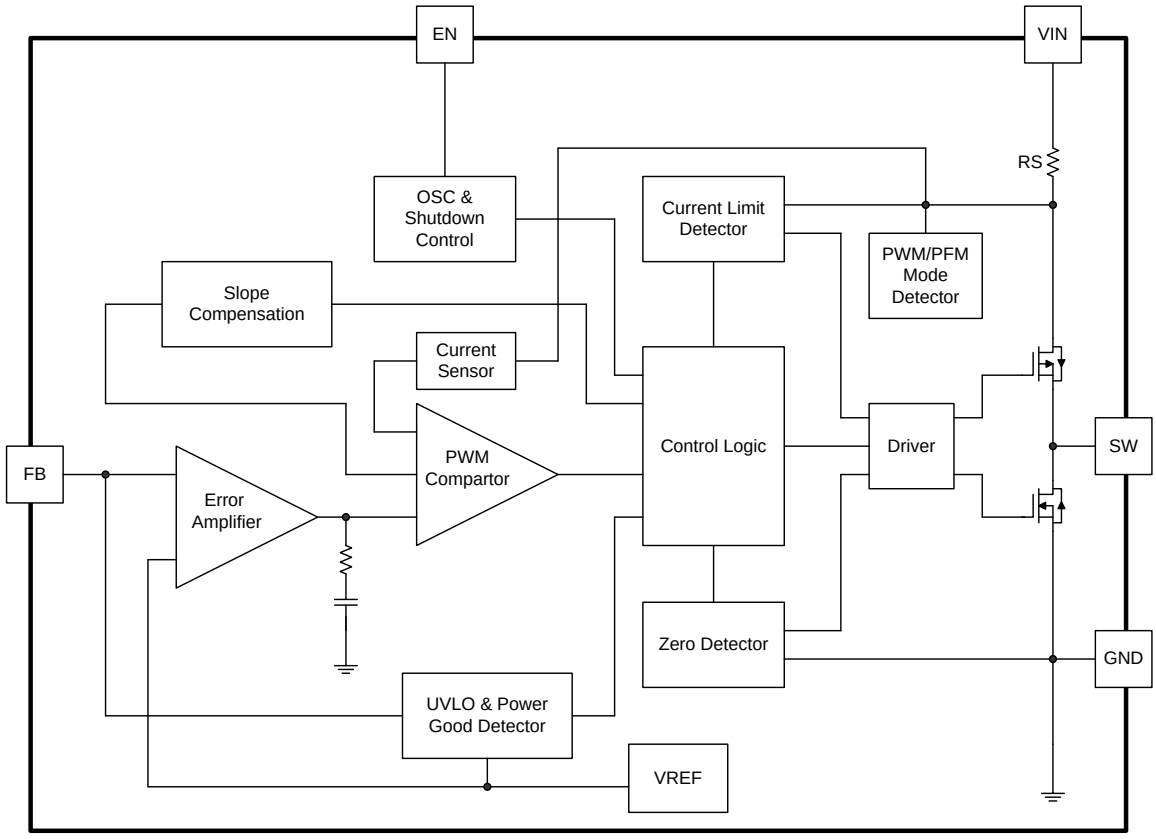
## Functional Block Diagram




Block Diagram

## Functions Description

### Internal Regulator

The PT62568 is a current mode step down DC/DC converter that provides excellent transient response with no extra external compensation components. This device contains an internal, low resistance, high voltage power MOSFET, and operates at a high 1.5MHz operating frequency to ensure a compact, high efficiency design with excellent AC and DC performance.

### Error Amplifier

The error amplifier compares the FB pin voltage with the internal FB reference (VFB) and outputs a current proportional to the difference between the two. This output current is then used to charge or discharge the internal compensation network, which is used to control the power MOSFET current. The optimized internal compensation network minimizes the external component counts and simplifies the control loop design.

### Internal Soft-Start

The soft-start is implemented to prevent the converter output voltage from overshooting during startup. When the chip starts, the internal circuitry generates a soft-start voltage (SS) ramping up from 0V to 0.6V. When it is lower than the internal reference (REF), SS overrides REF so the error amplifier uses SS as the reference. When SS is higher than REF, REF regains control. The SS time is internally max to 1.2ms.

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### Over Current Protection & Hiccup

The PT62568 has cycle-by-cycle over current limit when the inductor current peak value exceeds the set current limit threshold. Meanwhile, output voltage starts to drop until FB is below the Under-Voltage (UV) threshold, typically 25% below the reference. Once a UV is triggered, the PT62568 enters hiccup mode to periodically restart the part. This protection mode is especially useful when the output is dead-short to ground. The average short circuit current is greatly reduced to alleviate the thermal issue and to protect the regulator. The PT62568 exits the hiccup mode once the over current condition is removed.

### Startup and Shutdown

If both VIN and EN are higher than their appropriate thresholds, the chip starts. The reference block starts first, generating stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides stable supply for the remaining circuitries. Three events can shut down the chip: EN low, VIN low and thermal shutdown. In the shutdown procedure, the signaling path is first blocked to avoid any fault triggering. The comp voltage and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

## Applications Information

### Setting the Output Voltage

PT62568 require an input capacitor, an output capacitor and an inductor. These components are critical to the performance of the device. PT62568 are internally compensated and do not require external components to achieve stable operation. The output voltage can be programmed by resistor divider.

$$V_{OUT} = V_{FB} \times \frac{R1 + R2}{R2}$$

| $V_{OUT}$ | R1 | R2 | $L1_{MIN}$ | $L1_{TYP}$ | $L1_{MAX}$ | $C_{IN}$ | $C_{OUT}$ | $C_{FF}$ Opt. |
|---|---|---|---|---|---|---|---|---|
| 1.05V | 7.5KΩ | 10KΩ | 1.0μH | 2.2μH | 4.7μH | 20-47uF | 20-68uF | 20-1000pF |
| 1.2V | 10KΩ | 10KΩ | 1.0μH | 2.2μH | 4.7μH | 20-47uF | 20-68uF | 20-1000pF |
| 1.5V | 15KΩ | 10KΩ | 1.0μH | 2.2μH | 4.7μH | 20-47uF | 20-68uF | 20-1000pF |
| 3.3V | 45KΩ | 10KΩ | 1.0μH | 4.7μH | 6.8μH | 20-47uF | 20-68uF | 20-1000pF |

### Selecting the Inductor

The recommended inductor values are shown in the Application Diagram. It is important to guarantee the inductor core does not saturate during any foreseeable operational situation. The inductor should be rated to handle the peak load current plus the ripple current: Care should be taken when reviewing the different saturation current ratings that are specified by different manufacturers. Saturation current ratings are typically specified at 25°C, so ratings at maximum ambient temperature of the application should be requested from the manufacturer.

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times F_{OSC}}$$

Where ΔIL is the inductor ripple current. Choose inductor ripple current to be approximately 30% if the maximum

load current. The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Under light load conditions below 100mA, larger inductance is recommended for improved efficiency.

## Selecting the Output Capacitor

Special attention should be paid when selecting these components. The DC bias of these capacitors can result in a capacitance value that falls below the minimum value given in the recommended capacitor specifications table.
The ceramic capacitor's actual capacitance can vary with temperature. The capacitor type X7R, which operates over a temperature range of −55°C to +125°C, will only vary the capacitance to within ±15%. The capacitor type X5R has a similar tolerance over a reduced temperature range of −55°C to +85°C. Many large value ceramic capacitors, larger than 1uF are manufactured with Z5U or Y5V temperature characteristics. Their capacitance can drop by more than 50% as the temperature varies from 25°C to 85°C. Therefore X5R or X7R is recommended over Z5U and Y5V in applications where the ambient temperature will change significantly above or below 25°C.
Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 0.47uF to 44uF range. Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. It should also be noted that the ESR of a typical tantalum will increase about 2:1 as the temperature goes from 25°C down to −40°C, so some guard band must be allowed.

## PC Board Layout Consideration

PCB layout is very important to achieve stable operation. It is highly recommended to duplicate EVB layout for optimum performance. If change is necessary, please follow these guidelines for reference.

1. Keep the path of switching current short and minimize the loop area formed by Input capacitor, high-side MOSFET and low-side MOSFET.
2. Bypass ceramic capacitors are suggested to be put close to the Vin Pin.
3. Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close to the chip as possible.
4. VOUT, SW away from sensitive analog areas such as FB.

Connect IN, SW, and especially GND respectively to a large copper area to cool the chip to improve thermal performance and long-term reliability.

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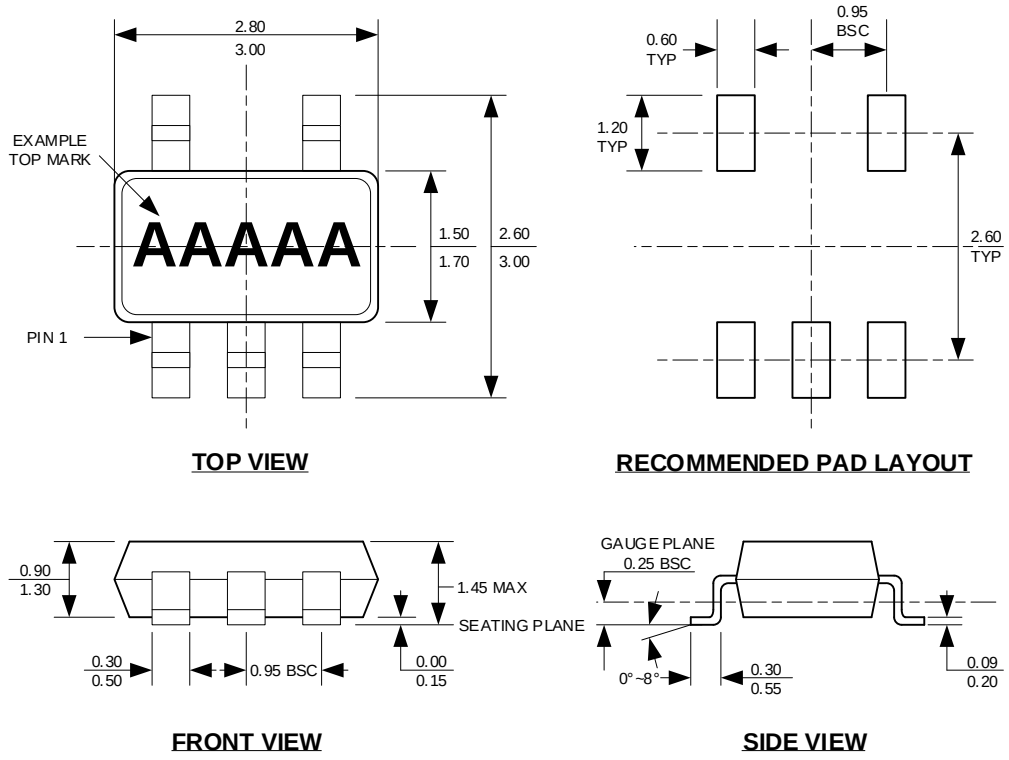
## Package Description

### SOT23-5




**NOTE:**
1. CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2. PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3. PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5. DRAWING CONFORMS TO JEDEC MS-012, VARIATION BA.
6. DRAWING IS NOT TO SCALE.